TA9210D – 12.5W CW, 30 – 4000 MHz GaN Power Transistor

1.0 Features

- Small signal gain @ 800 MHz: 18 dB
- Large signal gain @ 800 MHz: 13.5 dB
- PSAT @ 800 MHz: 41.5 dBm
- PAE @ PSAT @ 800 MHz: >55%
- 28 – 32 V Typical operations
- Operating frequency: 30 MHz to 4.0 GHz

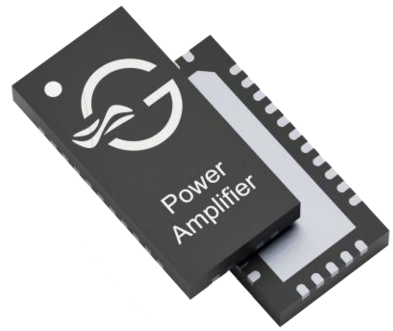

Figure 1.1 Device Image
(32 Pin 3 × 6 × 0.75 mm QFN Package)

RoHS/REACH/Halogen Free Compliance

2.0 Applications

- Private mobile radio handsets
- Public safety radios
- Cellular infrastructure
- Military radios

3.0 Description

The TA9210D is a broadband capable 12.5W GaN power transistor covering 30 MHz to 4.0 GHz frequency band with a single match. The input and output can be matched for best power and efficiency for the desired band.

The TA9210D is packaged in a compact, low-cost Quad Flat No lead (QFN) 3 x 6 x 0.75 mm^3, 32 leads plastic package.

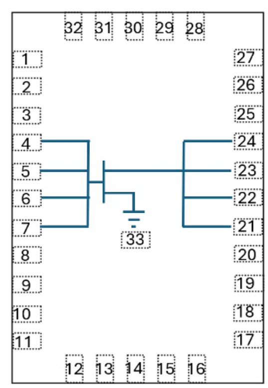

Figure 3.1 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 4.1 Ordering Information

Device Part Number	Package Type	Notes
TA9210D	32 Pin 3.0×6.0×0.75 mm^3 QFN	Core part number
TA9210D-EVB-nn	Evaluation Board, see below	EVBs offered with different matchings
TA9210DMTRPBF	330mm reel, 3 000 pcs	Full Reel

Matching frequency range	Order code
Tuned Evaluation Board, 30 – 2600 MHz	TA9210D-EVB-A
Tuned Evaluation Board, 30 – 1000 MHz	TA9210D-EVB-A2
Tuned Evaluation Board, 1800 – 2700 MHz	TA9210D-EVB-B
Tuned Evaluation Board, 30 – 512 MHz	TA9210D-EVB-C
Tuned Evaluation Board, 30 – 1000 MHz	TA9210D-EVB-D
Tuned Evaluation Board, 30 – 1000 MHz (Resilient LNA)	TA9210D-EVB-D2
Tuned Evaluation Board, 30 – 512 MHz	TA9210D-EVB-E
Tuned Evaluation Board, 200 – 2700 MHz	TA9210D-EVB-F
Tuned Evaluation Board, 700 – 3700 MHz	TA9210D-EVB-G
Tuned Evaluation Board, 1200 – 2600 GHz	TA9210D-EVB-H
Tuned Evaluation Board, 3300 – 3800 MHz	TA9210D-EVB-I
Tuned Evaluation Board, 3000 – 3500 MHz	TA9210D-EVB-J
Tuned Evaluation Board, 2100 – 2500 MHz	TA9210D-EVB-K
Tuned Evaluation Board, 2400 – 2500 MHz	TA9210D-EVB-L
Tuned Evaluation Board, 200 – 2000 MHz	TA9210D-EVB-M
Tuned Evaluation Board, 135-870 MHz	TA9210D + TS7441L-EVB-K VHF
	TA9210D + TS7441L-EVB-K UHF1
	TA9210D + TS7441L-EVB-K UHF2
	TA9210D + TS7441L-EVB-K 800 MHz

5.0 Pin Description

Table 5.1 Pin Definition

Pin Number	Pin Name	Description
1, 2, 3, 9, 10, 11, 17, 18, 19, 25, 26, 27	NC	No internal connection. Can be grounded
12, 13, 14, 15, 16, 28, 29, 30, 31, 32	GND	No internal connection. Pins should be grounded and connected to the GND slug for improved thermal relief
4, 5, 6, 7, 8	V_{GG} & RF_{IN}	Gate voltage and RF input
20, 21, 22, 23, 24	V_{DD} & RF_{OUT}	Drain voltage and RF output
33[1]	Paddle/Slug	Ground

Note: [1] The backside ground slug of the device must be grounded directly to the ground plane through multiple vias to ensure proper operation. Adequate heat sinking required.

6.0 Absolute Maximum Ratings

Table 6.1 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Breakdown voltage	V_{DS}	+120	V
Gate voltage	V_{GS}	-30 to +2.0	V
Drain current	I_{DS}	1.5	A
Gate current	I_{GS}	4	mA
Power dissipation CW	P_{diss}	22	W
RF input power CW, @800 MHz	RF_{IN}	30	dBm
Storage Temperature Range	T_{st}	-55 to +150	°C
Operating Temperature Range	T_{op}	-40 to +85	°C
Maximum Junction Temperature	T_J	+225	°C
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{θJC}$	6.5	°C/W
Thermal Resistance (junction-to-top)	$R_{θJT}$	40	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C2A	500 to <750	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 RF Electrical Specifications

Table 7.1 Electrical Specifications @T_A=+25°C Unless otherwise specified

Parameter	Condition	Minimum	Typical	Maximum	Unit
Small Signal Gain	800 MHz		18		dB
Large Signal Gain	P_{OUT} = 41 dBm, 800 MHz		13.5		dB
P_{SAT}	800 MHz		41.5		dBm
Power Added Efficiency (PAE)	P_{OUT} = 41 dBm		54		%
Drain Voltage			32		V
Ruggedness	All phase, P_{OUT} = 41 dBm	VSWR = 10:1			

Note: Data taken from 30 – 2600 MHz broadband reference design (EVB), V_D=+32 V; I_{DQ}=50 mA, CW

8.0 Recommended Operating Conditions

Table 8.1 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Drain Voltage	V_{DD}	+12	+32	+34	V
Gate Voltage	V_{GG}	-2.7	-2.52	-2.3	V
Drain Bias Current	I_{DQ}		50		mA
Drain Current	I_{DS}		700		mA
Power Dissipation CW [1]	P_{diss}			20	W
Operating Temperature Range		-40	+25	+85	°C

Note: [1] @TC = +85°C

9.0 Bias and Sequencing

Table 9.1 Bias and Sequencing

Turn ON Device	Turn OFF Device
1. Set V_G to -5 V 2. Set V_D to +28/32 V 3. Adjust V_G to reach required I_{DQ} current 4. Apply RF power	1. Turn RF power off 2. Turn off V_D 3. Turn off V_G

10.0 Typical Characteristics

10.1 30 – 2600 MHz EVB A (Vdd = 28 V)

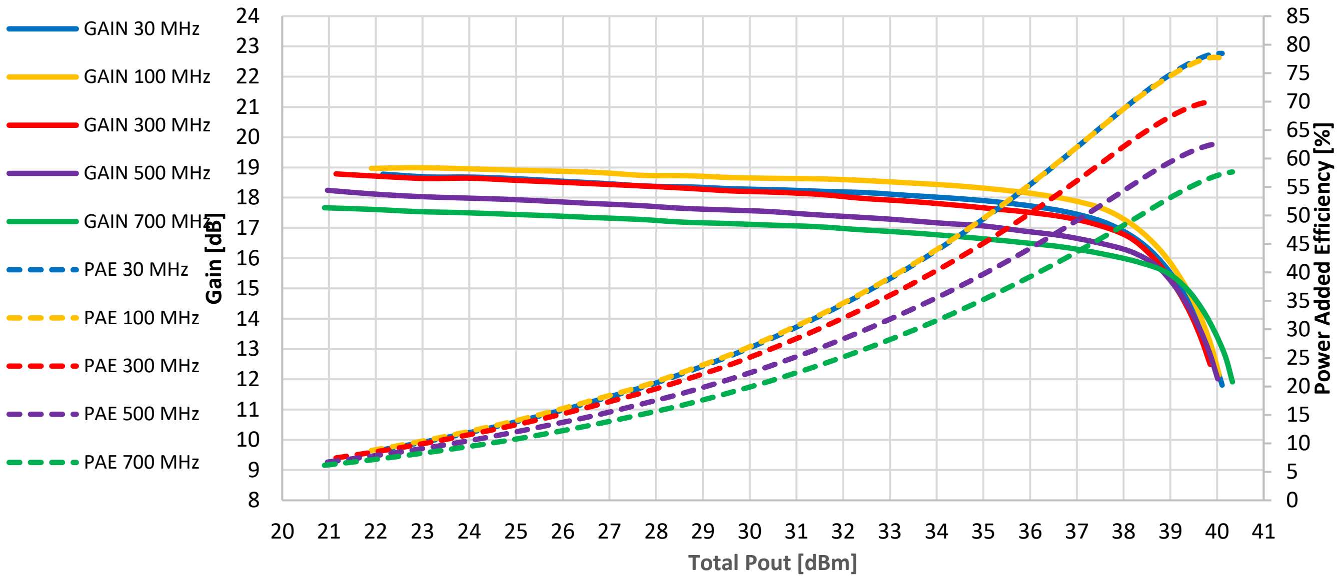

Figure 10.1.1 Gain and PAE vs P_{OUT} (30-700 MHz)
(V_D=28 V, I_{DQ}=50 mA, CW, T_A=+25°C)

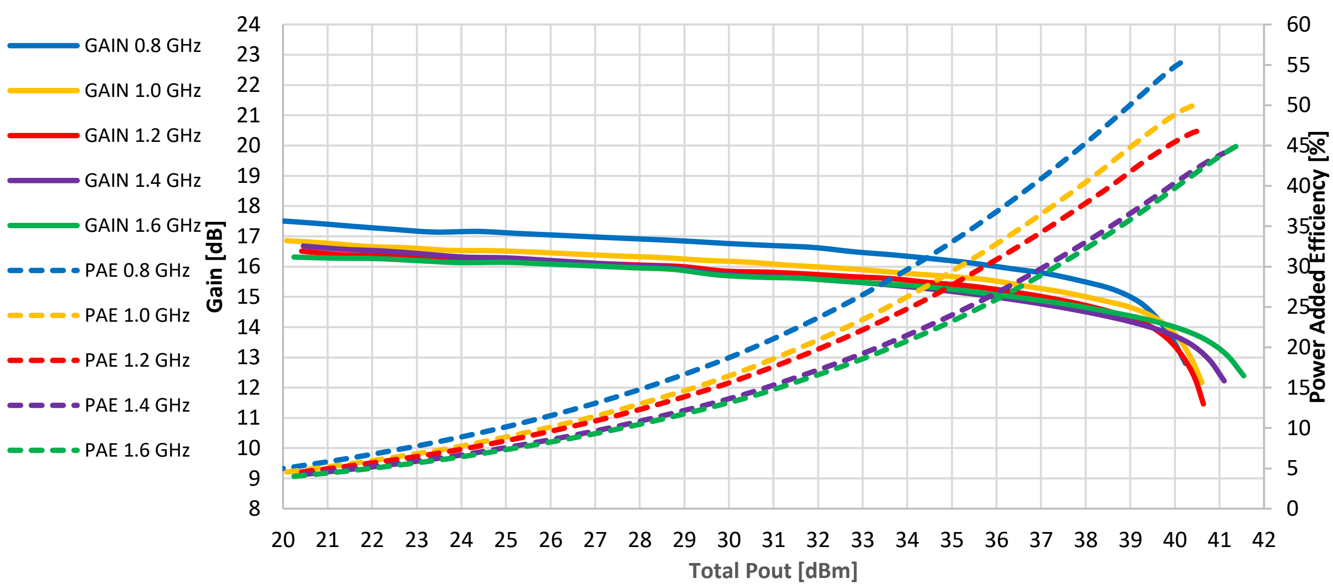

Figure 10.1.2 Gain and PAE vs P_{OUT} (800-1600 MHz)
(V_D=28 V, I_{DQ}=50 mA, CW, T_A=+25°C)

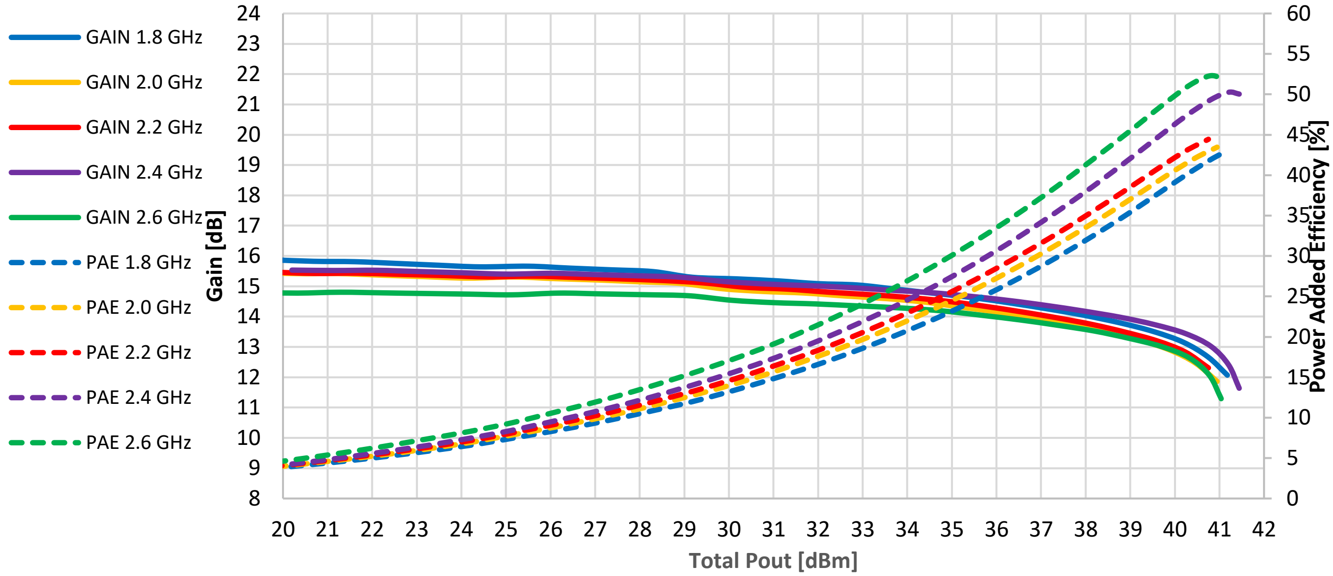

Figure 10.1.3 Gain and PAE vs P_{OUT} (1800-2600 MHz)

(V_D=28 V, I_{DQ}=50 mA, CW, T_A=+25°C)

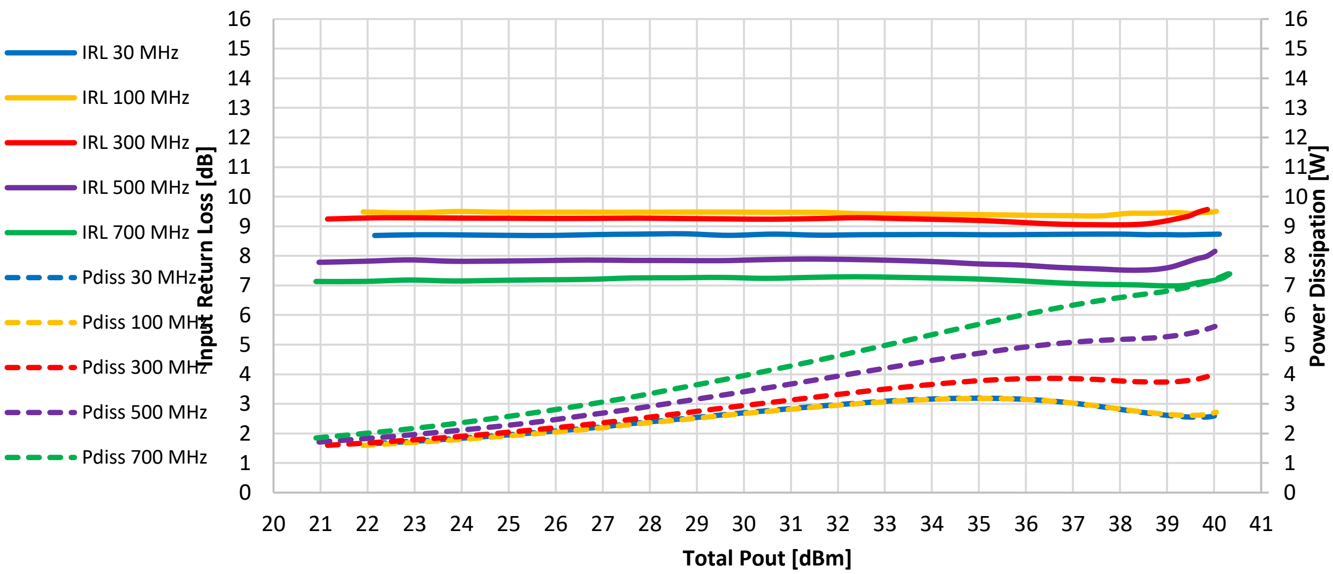

Figure 10.1.4 IRL and P_{diss} vs P_{OUT} (30-700 MHz)

(V_D=28 V, I_{DQ}=50 mA, CW, T_A=+25°C)

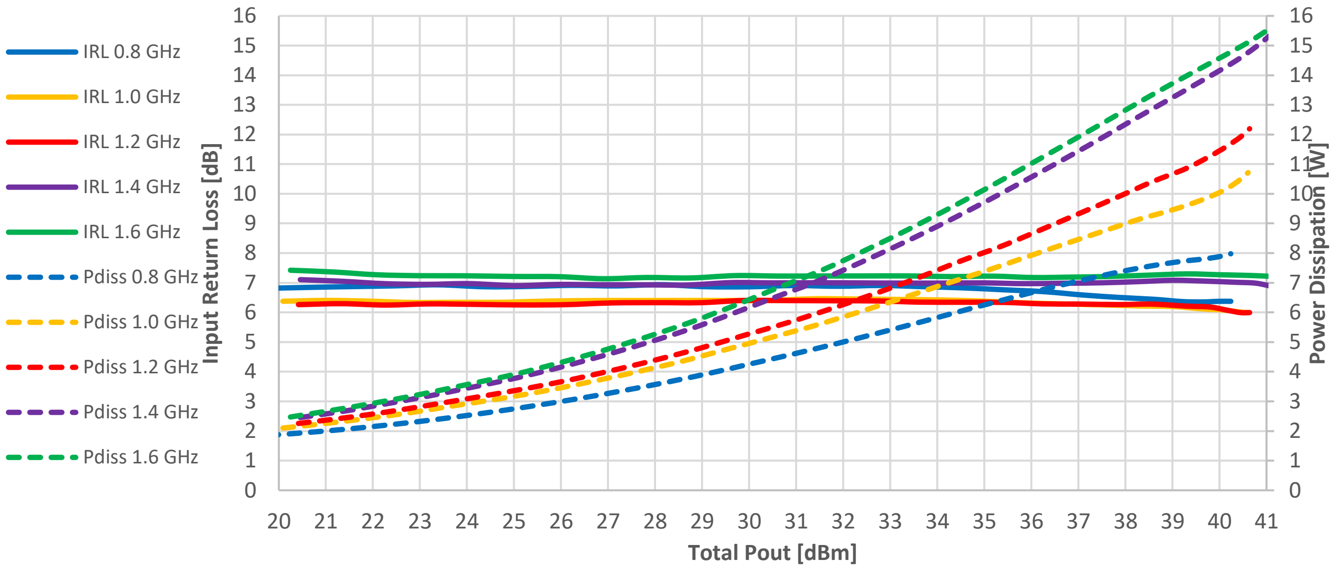

Figure 10.1.5 IRL 10and P_{diss} vs P_{OUT} (800-1600 MHz)
(V_D=28 V, I_{DQ}=50 mA, CW, T_A=+25°C)

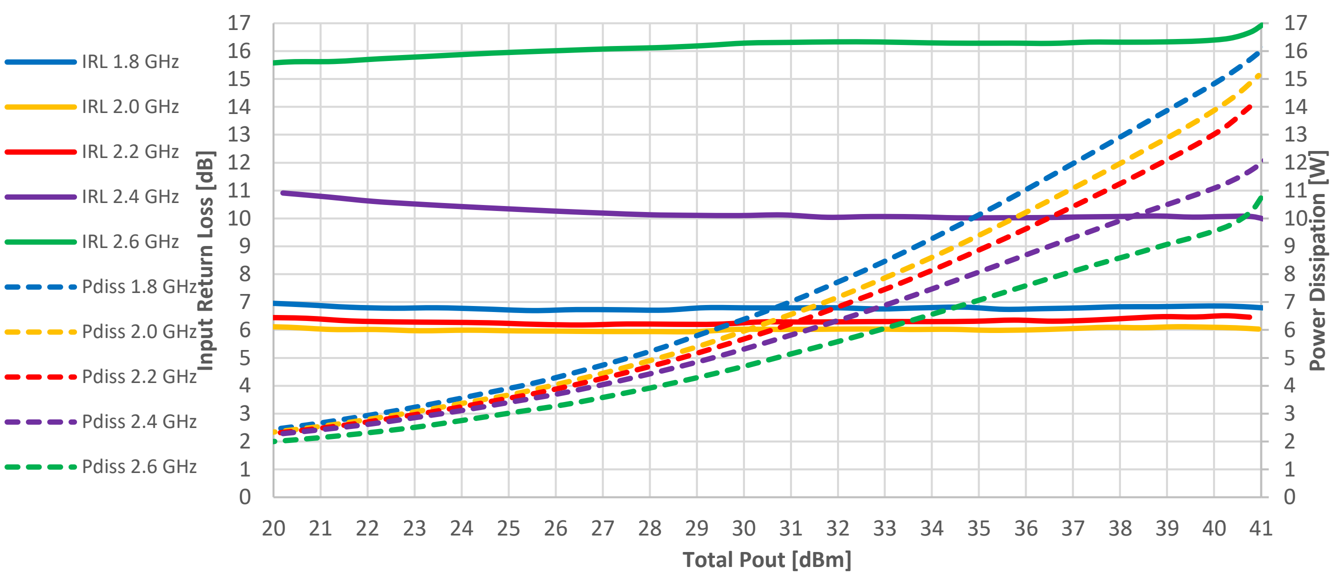

Figure 10.1.6 IRL and P_{diss} vs P_{OUT} (1800-2600 MHz)
(V_D=28 V, I_{DQ}=50 mA, CW, T_A=+25°C)

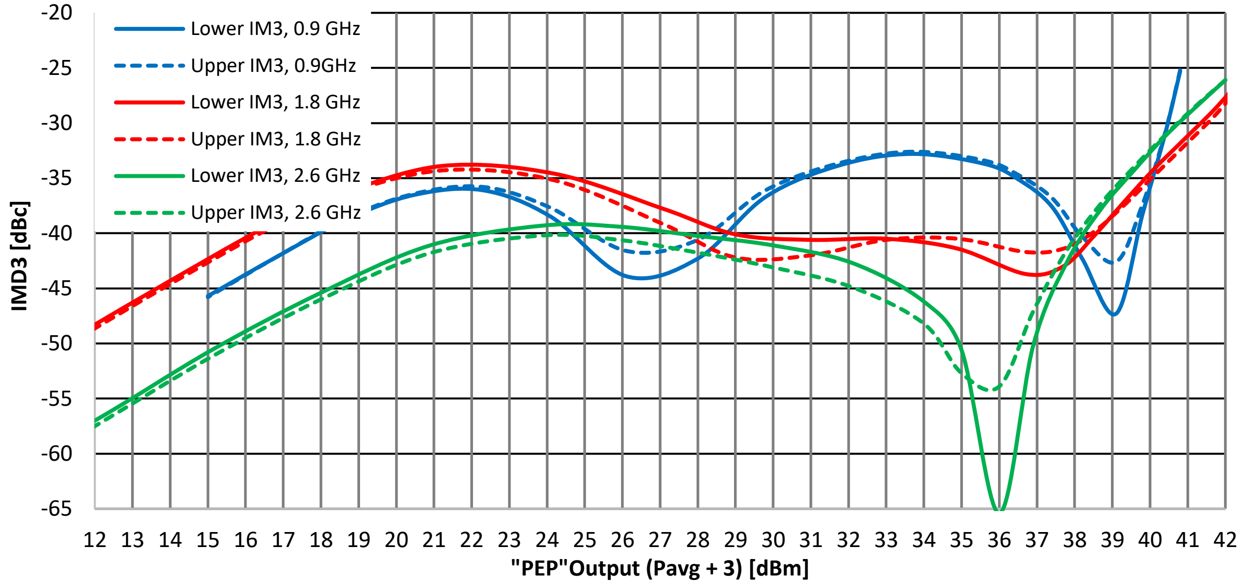

Figure 10.1.7 IMD3 vs P_{OUT}

(V_D=28 V, I_{DQ}=50 mA, CW, Fsp=200 kHz, T_A=+25°C)

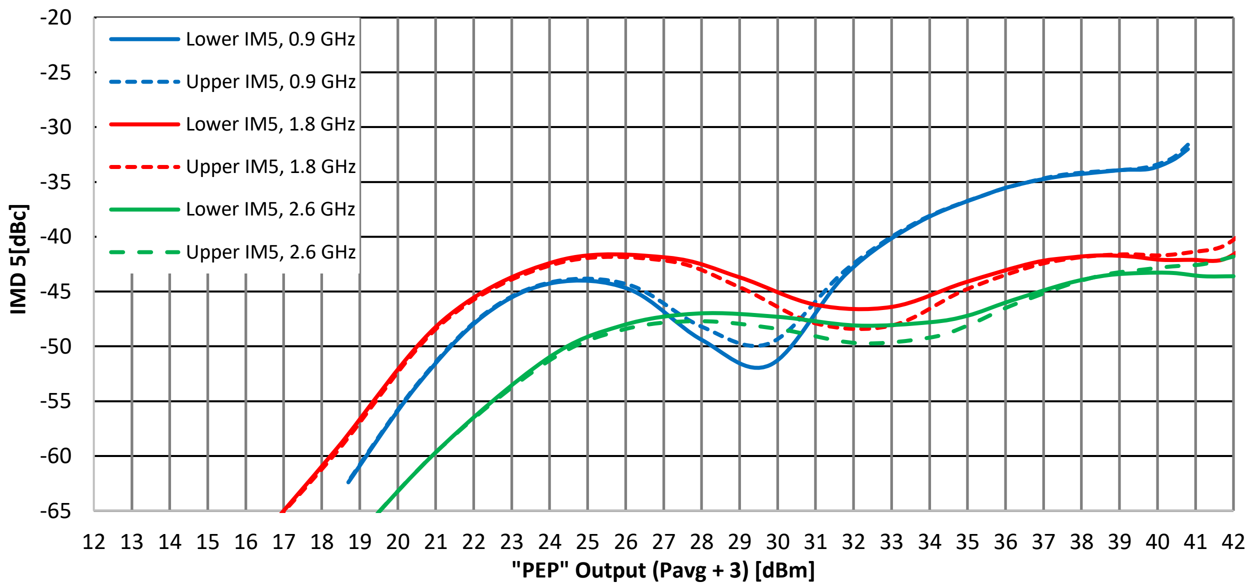

Figure 10.1.8 IMD5 vs P_{OUT}

(V_D=28 V, I_{DQ}=50 mA, CW, Fsp=200 kHz, T_A=+25°C)

10.2 30 - 2600MHz EVB A (Vdd = 32 V)

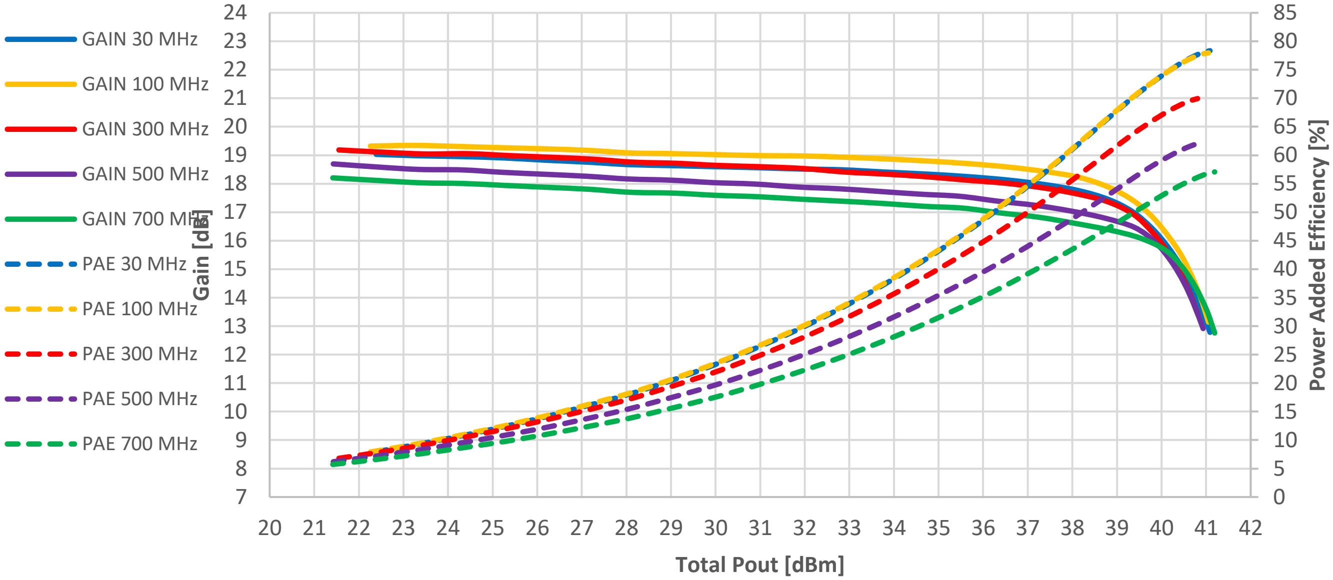

Figure 10.2.1 Gain and PAE vs P_{OUT} (30-700 MHz)
(V_D=32 V, I_{DQ}=50 mA, CW, T_A=+25°C)

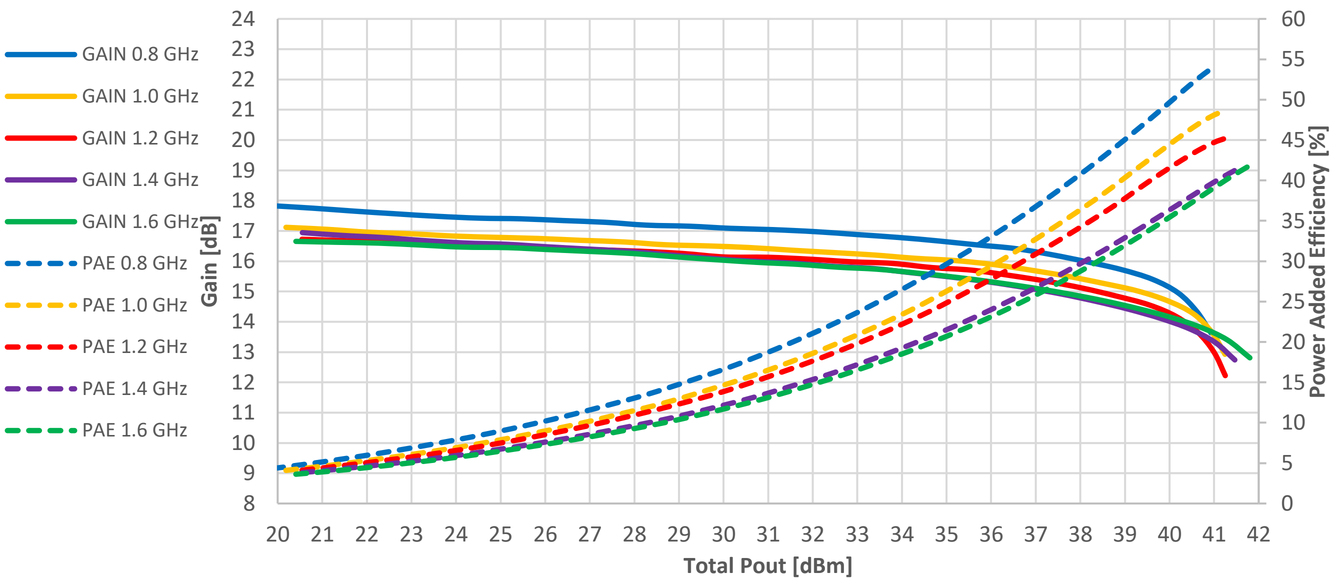

Figure 10.2.2 Gain and PAE vs P_{OUT} (800-1600 MHz)
(V_D=32 V, I_{DQ}=50 mA, CW, T_A=+25°C)

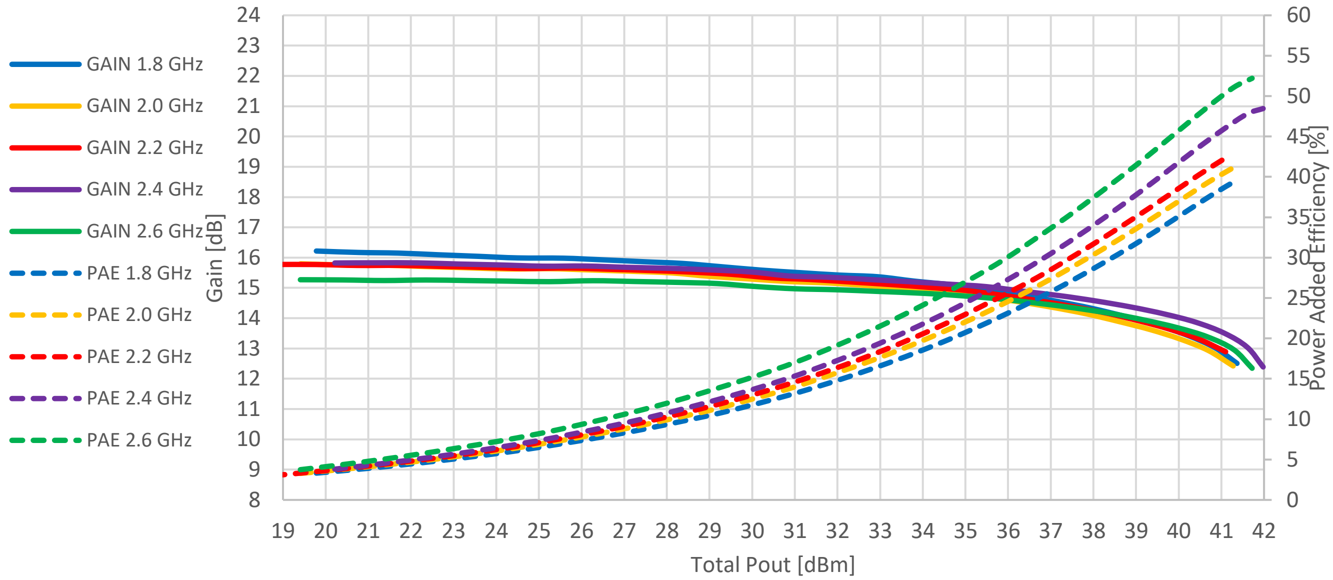

Figure 10.2.3 Gain and PAE vs P_{OUT} (1800-2600 MHz)

(V_D=32 V, I_{DQ}=50 mA, CW, T_A=+25°C)

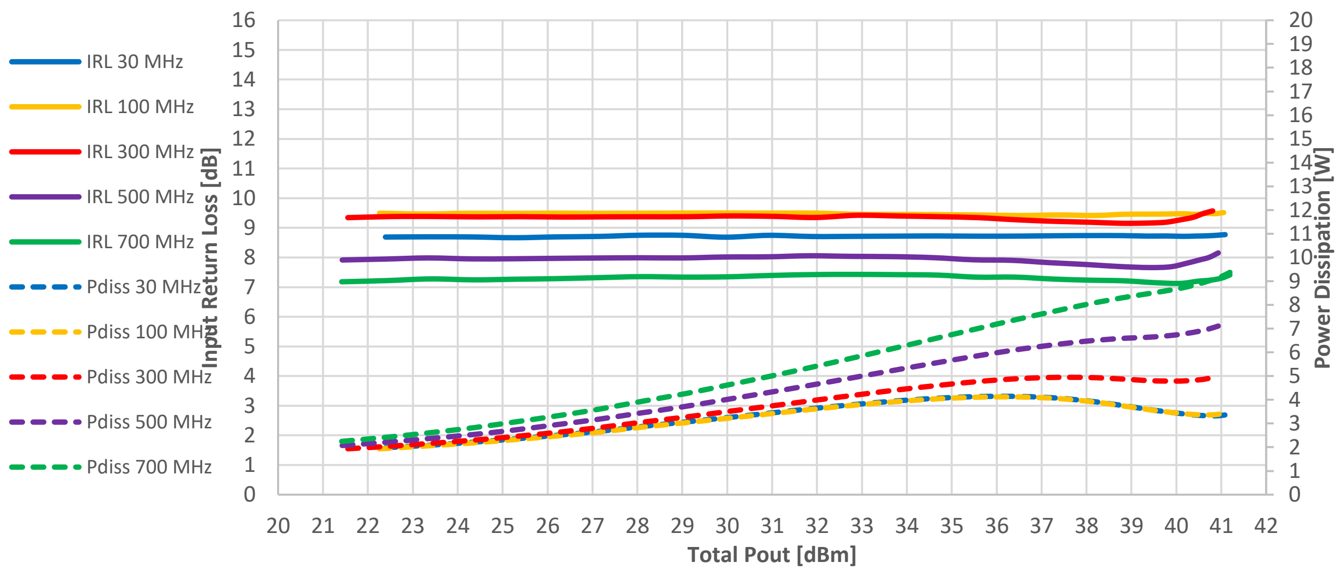

Figure 10.2.4 IRL and P_{diss} vs P_{OUT} (30-700 MHz)

(V_D=32 V, I_{DQ}=50 mA, CW, T_A=+25°C)

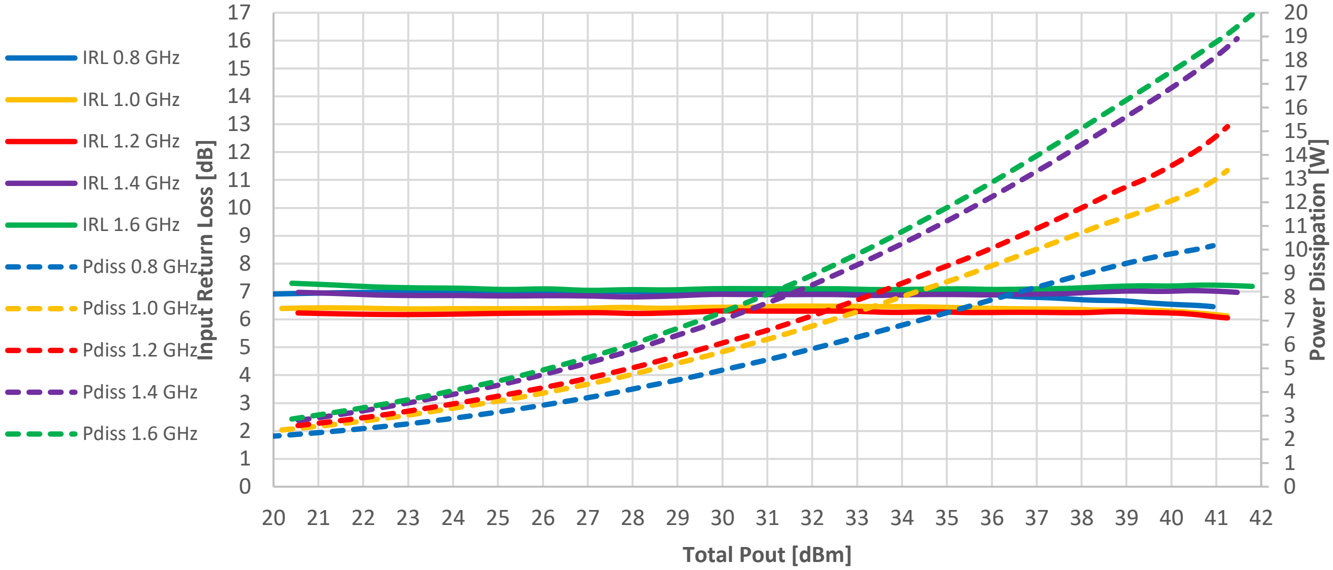

Figure 10.2.5 IRL and P_{diss} vs P_{OUT} (800-1600 MHz)

(V_D=32 V, I_{DQ}=50 mA, CW, T_A=+25°C)

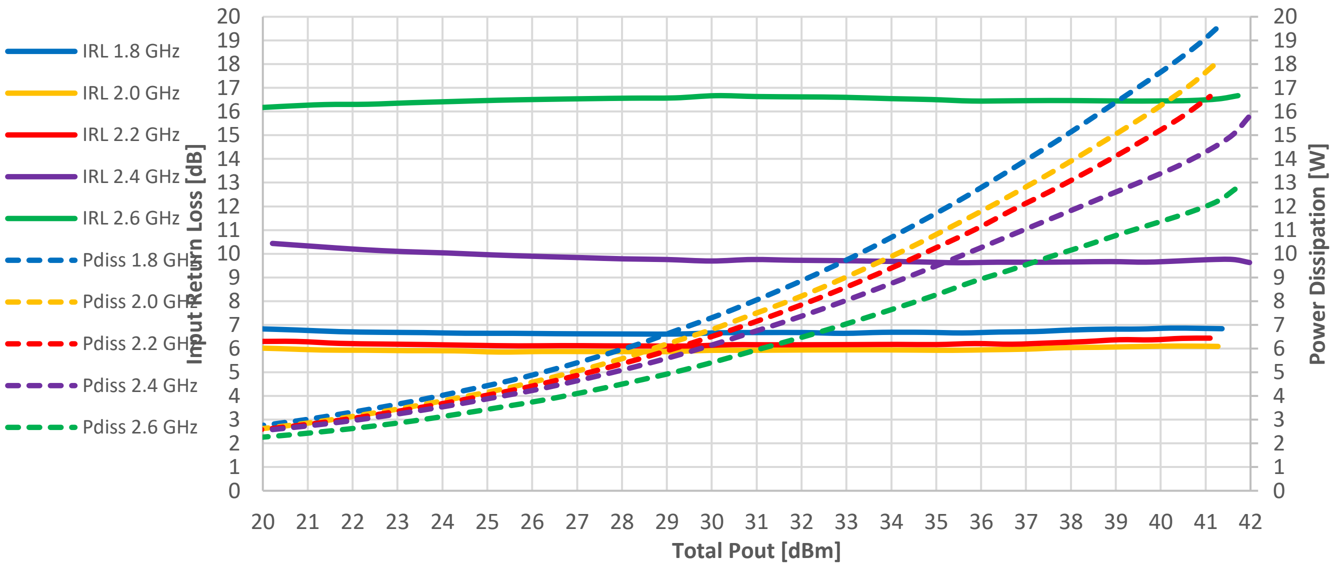

Figure 10.2.6 IRL and P_{diss} vs P_{OUT} (1800-2600 MHz)

(V_D=32 V, I_{DQ}=50 mA, CW, T_A=+25°C)

10.3 1.8 – 2.7 GHz EVB B (Vdd = 32 V)

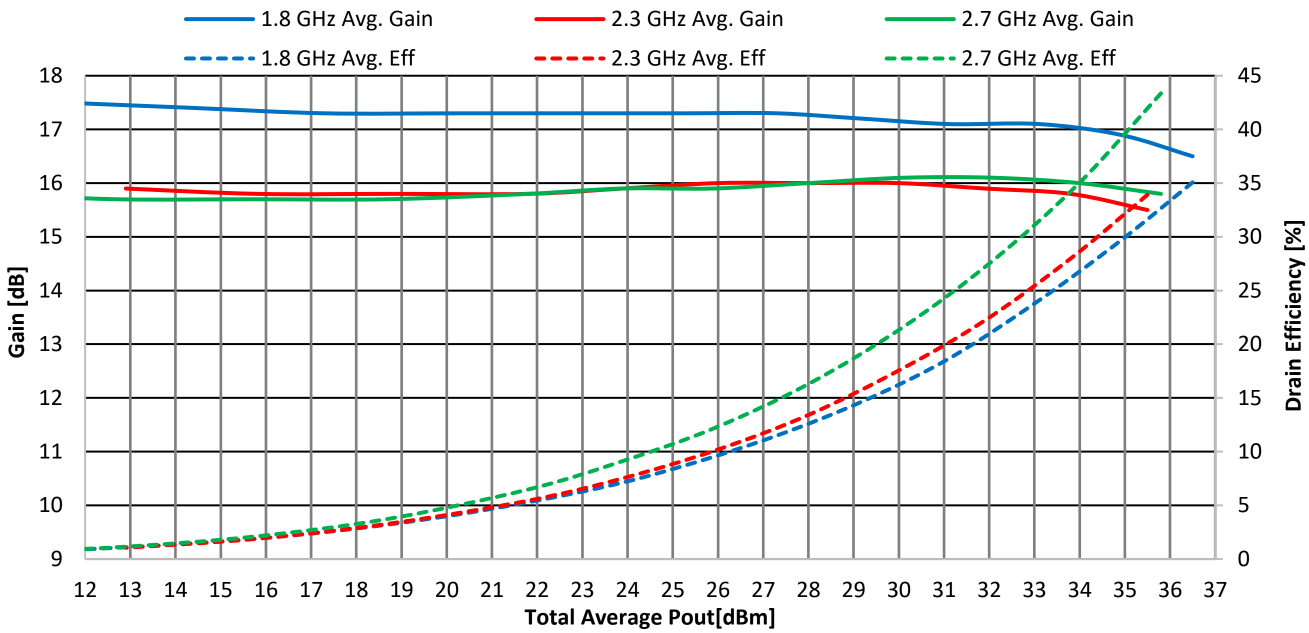

Figure 10.3.1 Gain and Efficiency vs P_{OUT}
(V_D=32 V, I_{DQ}=50 mA, LTE, PAPR = 9.5 dB, 10 MHz BW, T_A=+25°C)

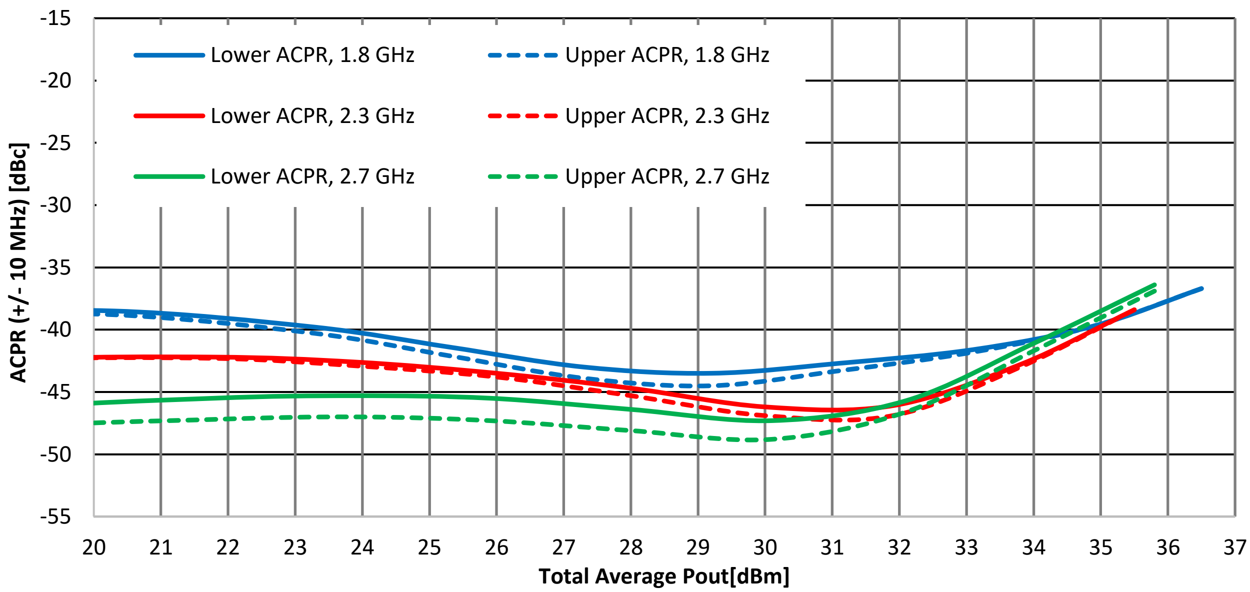

Figure 10.3.2 ACPR vs P_{OUT}
(V_D=32 V, I_{DQ}=50 mA, LTE, PAPR = 9.5 dB, 10 MHz BW, T_A=+25°C)

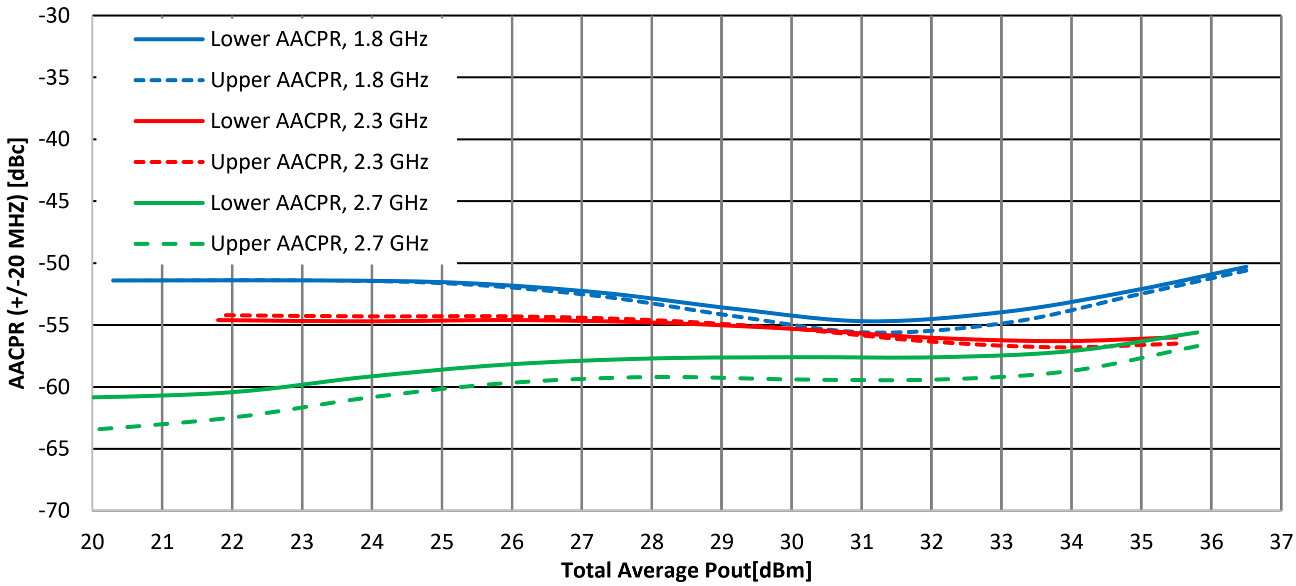

Figure 10.3.3 AACPR vs P_{OUT}

(V_D=32 V, I_{DQ}=50 mA, LTE, PAPR = 9.5 dB, 10 MHz BW, T_A=+25°C)

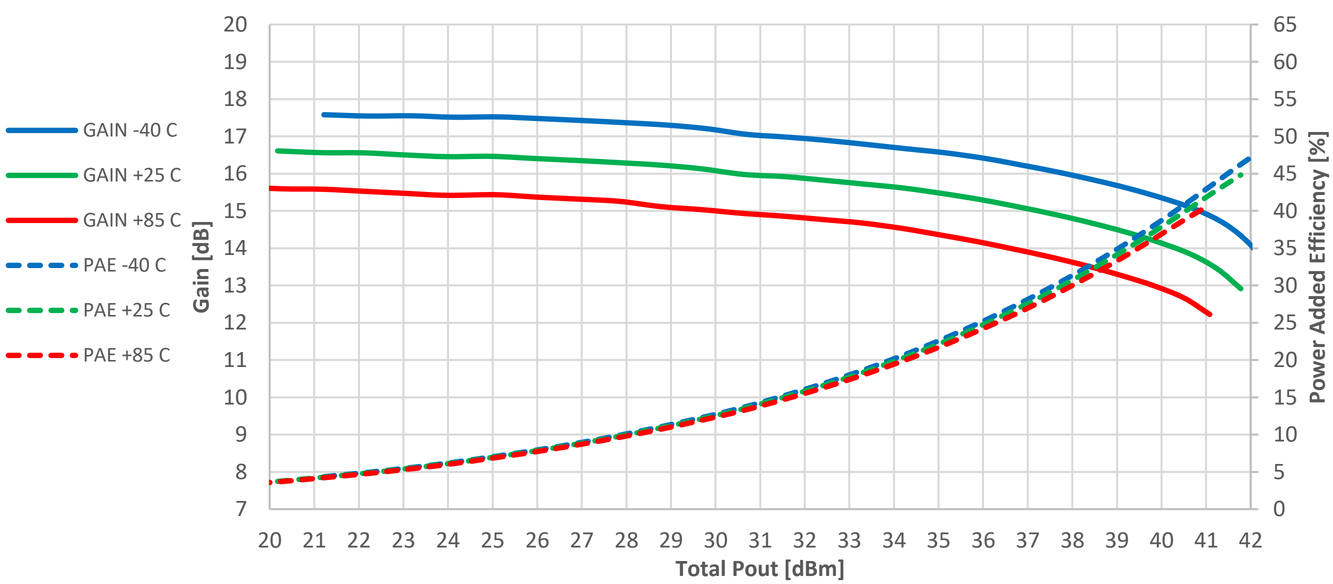

Figure 10.3.4 Gain and PAE vs P_{OUT} at 1.8 GHz over temp

(V_D=32 V, I_{DQ}=50 mA, CW)

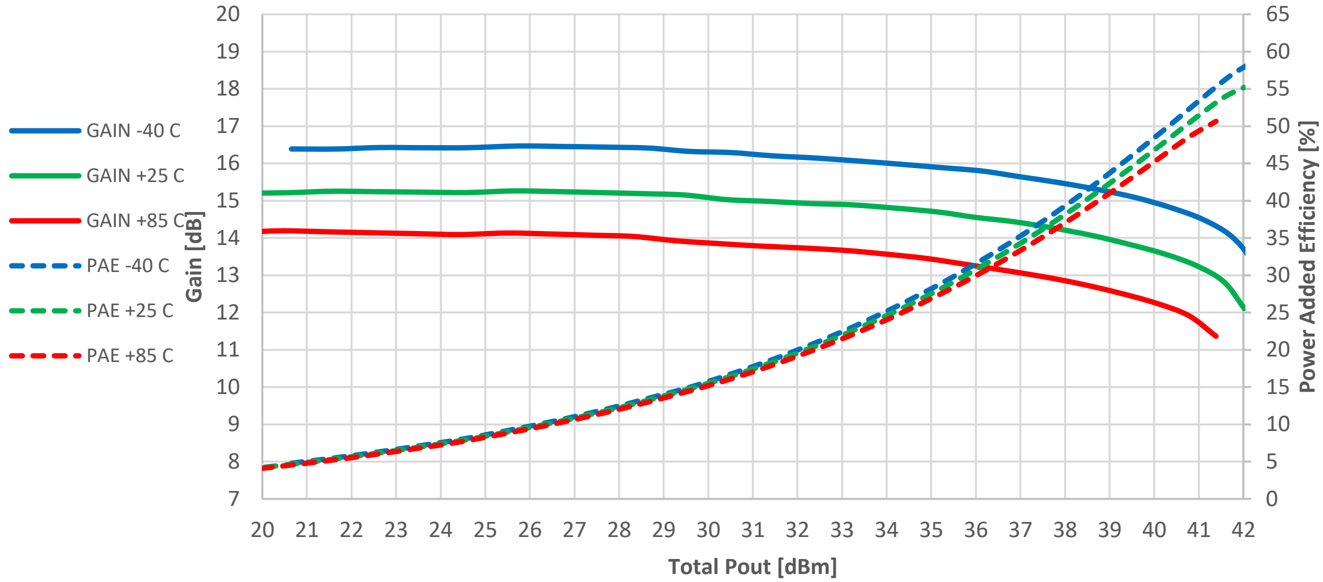

Figure 10.3.5 Gain and PAE vs P_{OUT} at 2.7 GHz over temp

(V_D=32 V, I_{DQ}=50 mA, CW)

11.0 Evaluation Boards

11.1 30 – 2600 MHz EVB A

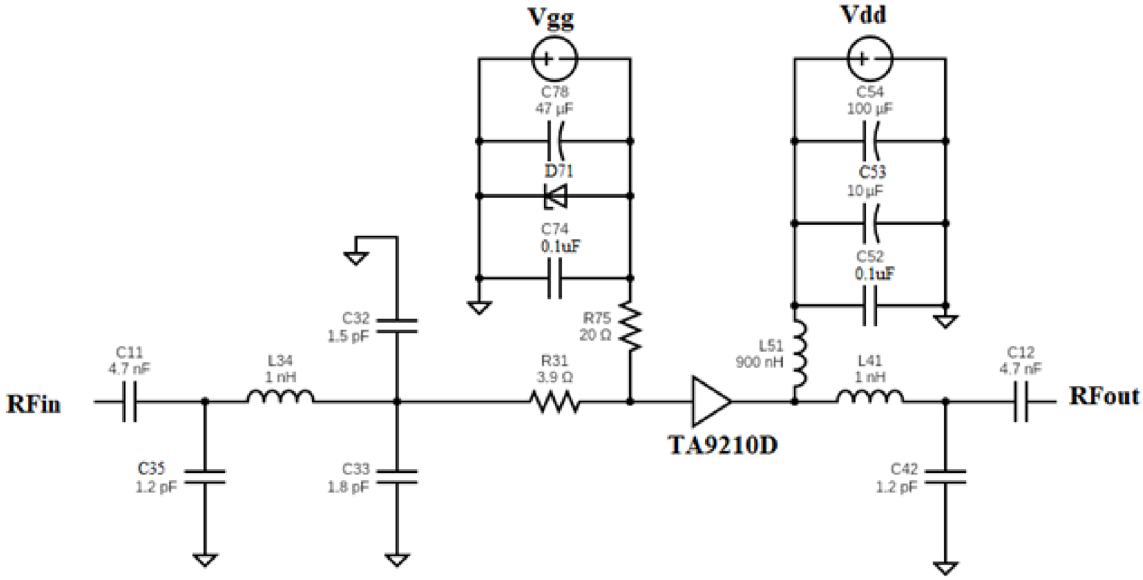

Figure 11.1.1 Schematic of the 30 – 2600 MHz EVB A

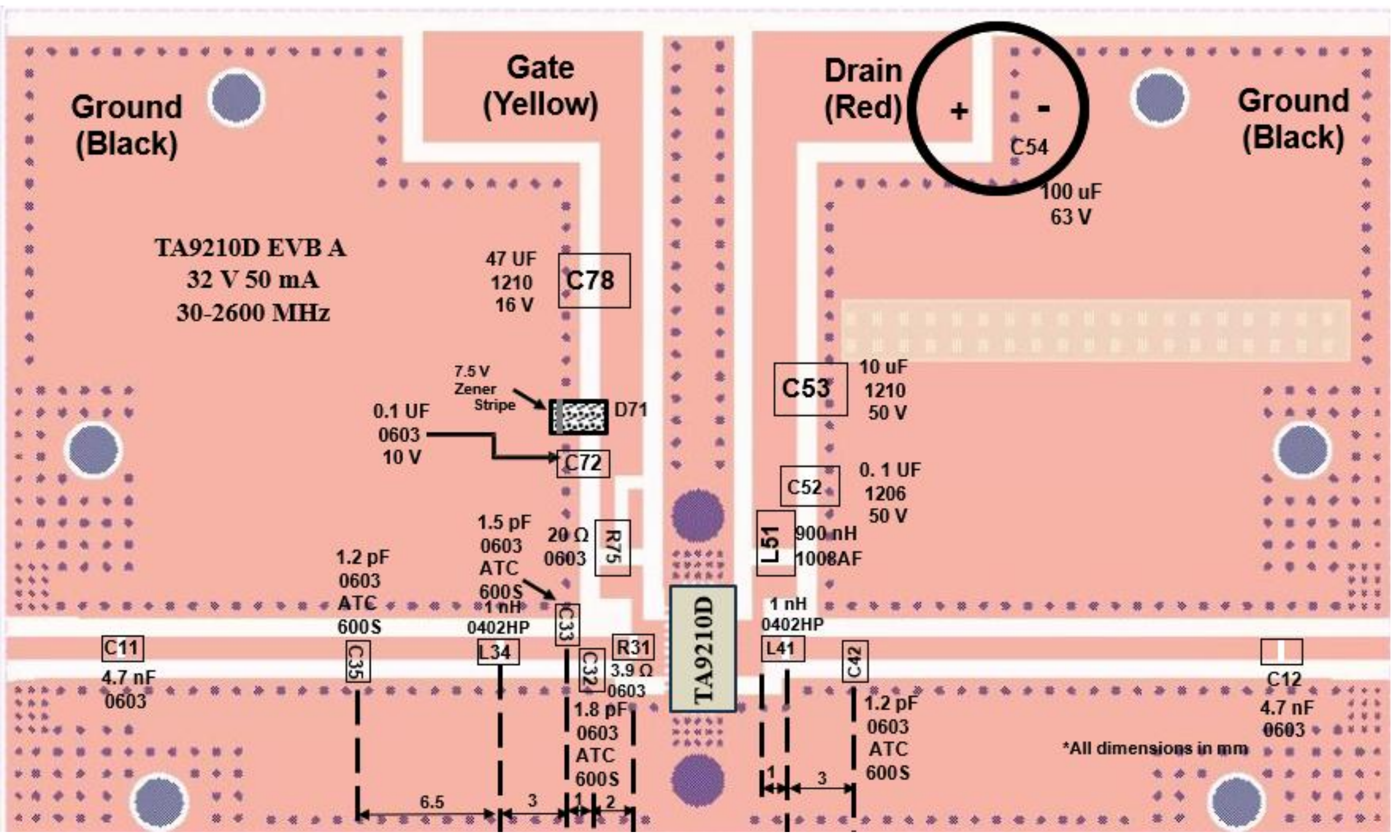

Figure 11.1.2 Board Layout of the 30 – 2600 MHz EVB A

Table 11.1.1 BOM of the 30 - 2600MHz EVB A

Component ID	Value	Manufacturer	Recommended Part Number
C11, C23	4.7 nF, 50V	Murata	GRM1885C1H472JA01
C12	1.2 pF	ATC	600S1R2CT250XT
L11, L22	1.0 nH	Coil craft	0402HP-1N0XGL
L21	900 nH	Coil craft	1008AF-901XJLC
C13	1.5 pF	ATC	600S1R5CT250XT
C14	1.8 pF	ATC	600S1R8CT250XT
C15	0.1 uF, 10 V	AVX	0603ZC104K4T2A
C21	0.1 uF, 50 V	Murata	GRM31C5C1H104JA01L
C22	1.2 pF	ATC	800A1R2BT250XT
C26	100 uF	Nichicon	UPW1J101MPD1TD
R11	3.9 Ω, 250 mW	Panasonic	ERJ-PA3J3R9V
R12	20 Ω, 250 mW	Panasonic	ERJ-PA3F20R0V
D11	7.5 V, 0.5 W Zener	On Semiconductor	SZMMSZ5236BT 1G
Q1	12.5 W GaN transistor	Tagore Tech	TA9210D
PCB	Rogers RO4350B, 20 mils, 2 oz copper		

11.2 1.8 - 2.7 GHz EVB B

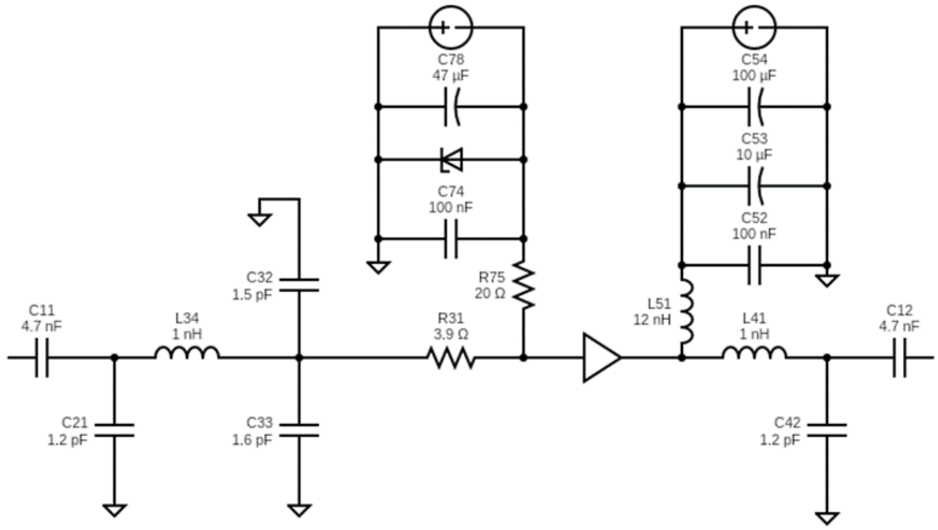

Figure 11.2.1 Schematic of the 1.8 - 2.7 GHz EVB B

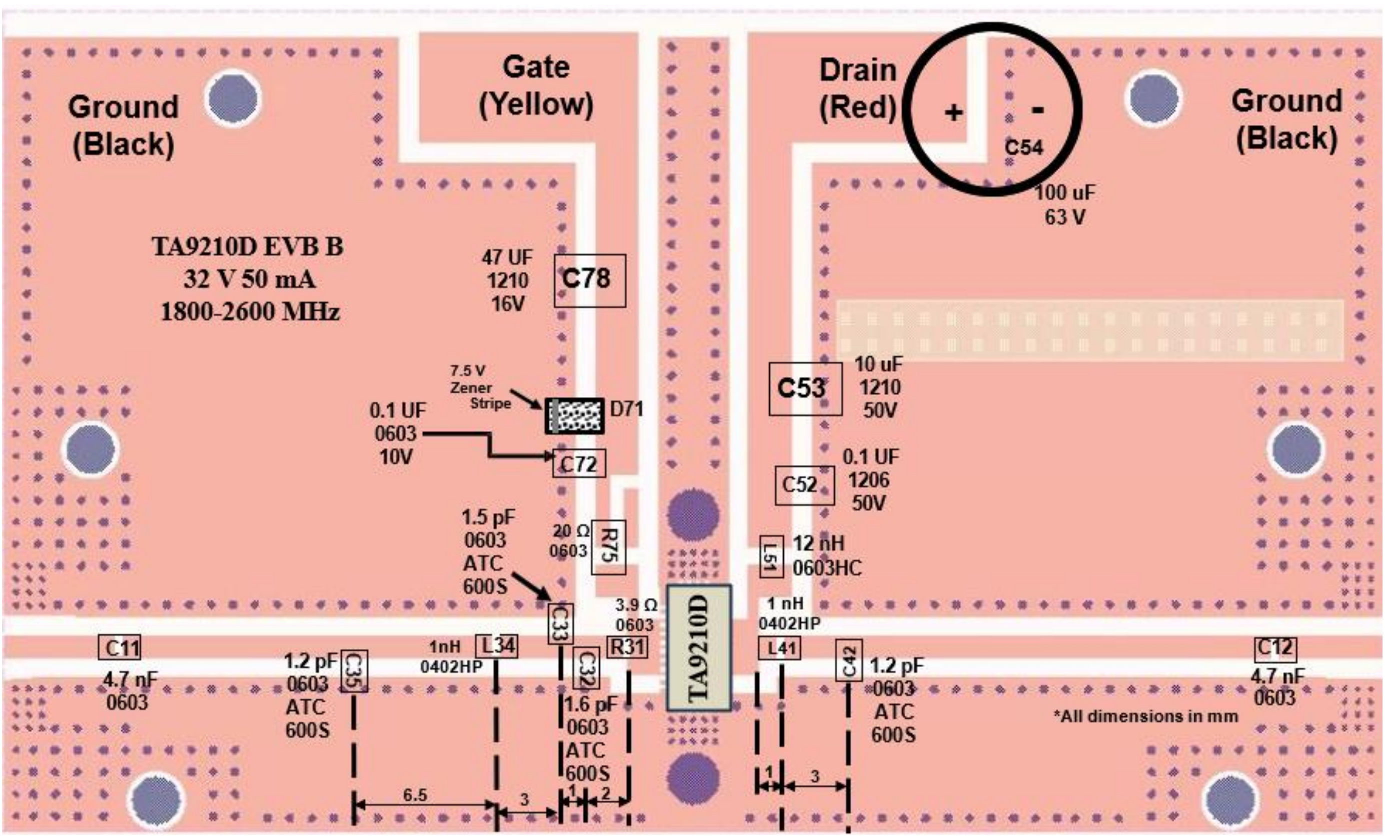

Figure 11.2.2 Board Layout of the 1.8 - 2.7 GHz EVB B

Table 11.2.1 BOM of the 1.8 – 2.7GHz EVB B

Component ID	Value	Manufacturer	Recommended Part Number
C11, C23	4.7 nF, 50 V	Murata	GRM1885C1H472JA01
C12	1.2 pF	ATC	600S1R2CT250XT
L11, L22	1.0 nH	Coil craft	0402HP-1N0XJL
L21	12 nH	Coil craft	0603HC-12NXGE
C13	1.5 pF	ATC	600S1R5CT250XT
C14	1.6 pF	ATC	600S1R6CT250XT
C15	0.1 uF, 10 V	AVX	0603ZC104K4T2A
C21	0.1 uF, 50 V	Murata	GRM31C5C1H104JA01L
C22	1.2 pF	ATC	800A1R2BT250XT
C26	100 uF	Nichicon	UPW1J101MPD1TD
R11	3.9 Ω, 250 mW	Panasonic	ERJ-PA3J3R9V
R12	20 Ω, 250 mW	Panasonic	ERJ-PA3F20R0V
D11	7.5 V, 0.5 W Zener	On Semiconductor	SZMMSZ5236BT 1G
Q1	12.5 W GaN transistor	Tagore Tech	TA9210D
PCB	Rogers RO4350B, 20 mils, 2 oz copper		

Note: Please refer to the application notes on our website for details about the EVBs mentioned above, as well as the additional EVBs listed in Table 4.1.

12.0 Device Package Information

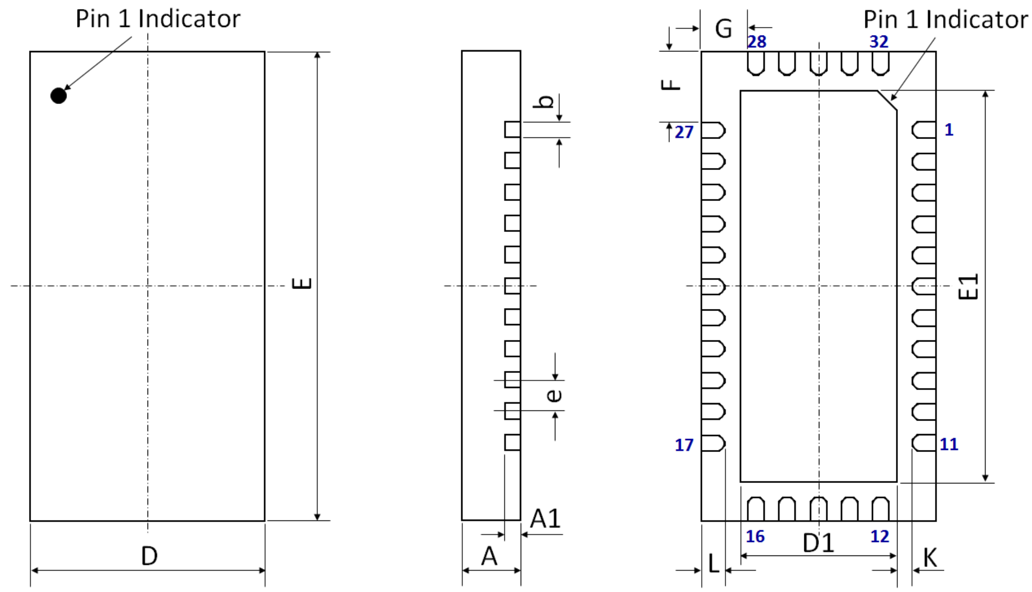

Figure 12.1 Device Package Drawing
(All dimensions are in mm)

Table 12.1 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.75	±0.05	E	6.00 BSC	±0.05
A1	0.203	±0.02	E1	5.00	±0.05
b	0.20	+0.05/-0.07	F	0.90	±0.05
D	3.00 BSC	±0.05	G	0.60	±0.05
D1	2.00	±0.05	L	0.25	±0.05
e	0.40 BSC	±0.05	K	0.25	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5 µm ~ 20 µm (Typical 10 µm ~ 12 µm)

Attention:
Please refer to application notes *TN-001* and *TN-002* at http://www.tagoretech.com for PCB and soldering related guidelines.

13.0 PCB Land Design

Guidelines:

[1] 2-layer PCB is recommended.

[2] Via diameter is recommended to be 0.2 mm to prevent solder wicking inside the vias.

[3] Thermal vias shall only be placed on the center pad.

[4] The maximum via number for the center pad is 4(X)×12(Y)=48.

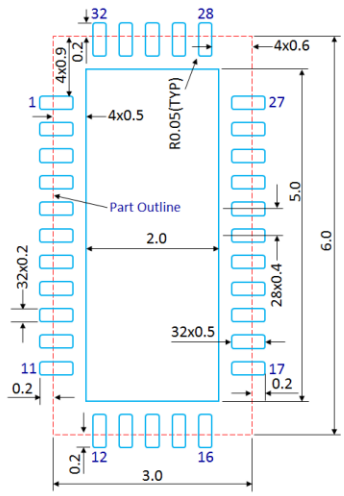

Figure 13.1 PCB Land Pattern

(Dimensions are in mm)

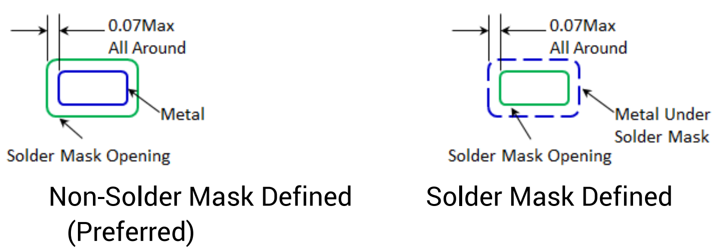

Figure 13.2 Solder Mask Pattern

(Dimensions are in mm)

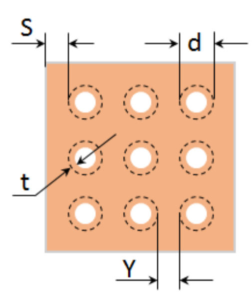

Figure 13.3 Thermal Via Pattern

(Recommended Values: S≥ 0.15 mm; Y≥ 0.20 mm; d= 0.2 mm; Plating Thickness t= 25 μm or 50 μm)

14.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125µm.

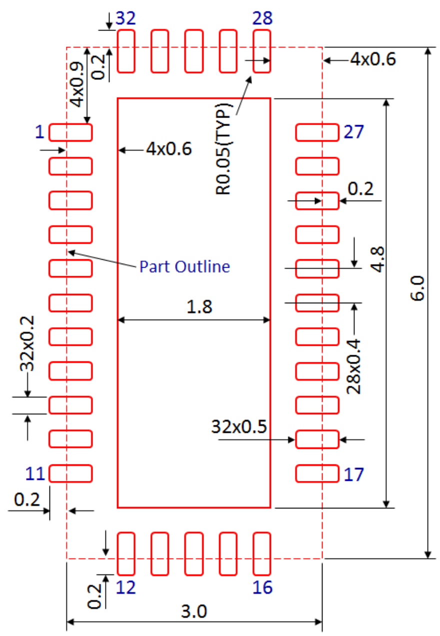

Figure 14.1 Stencil Openings
(Dimensions are in mm)

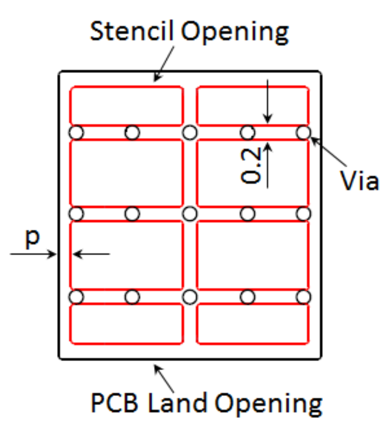

Figure 14.2 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

15.0 Tape and Reel Information

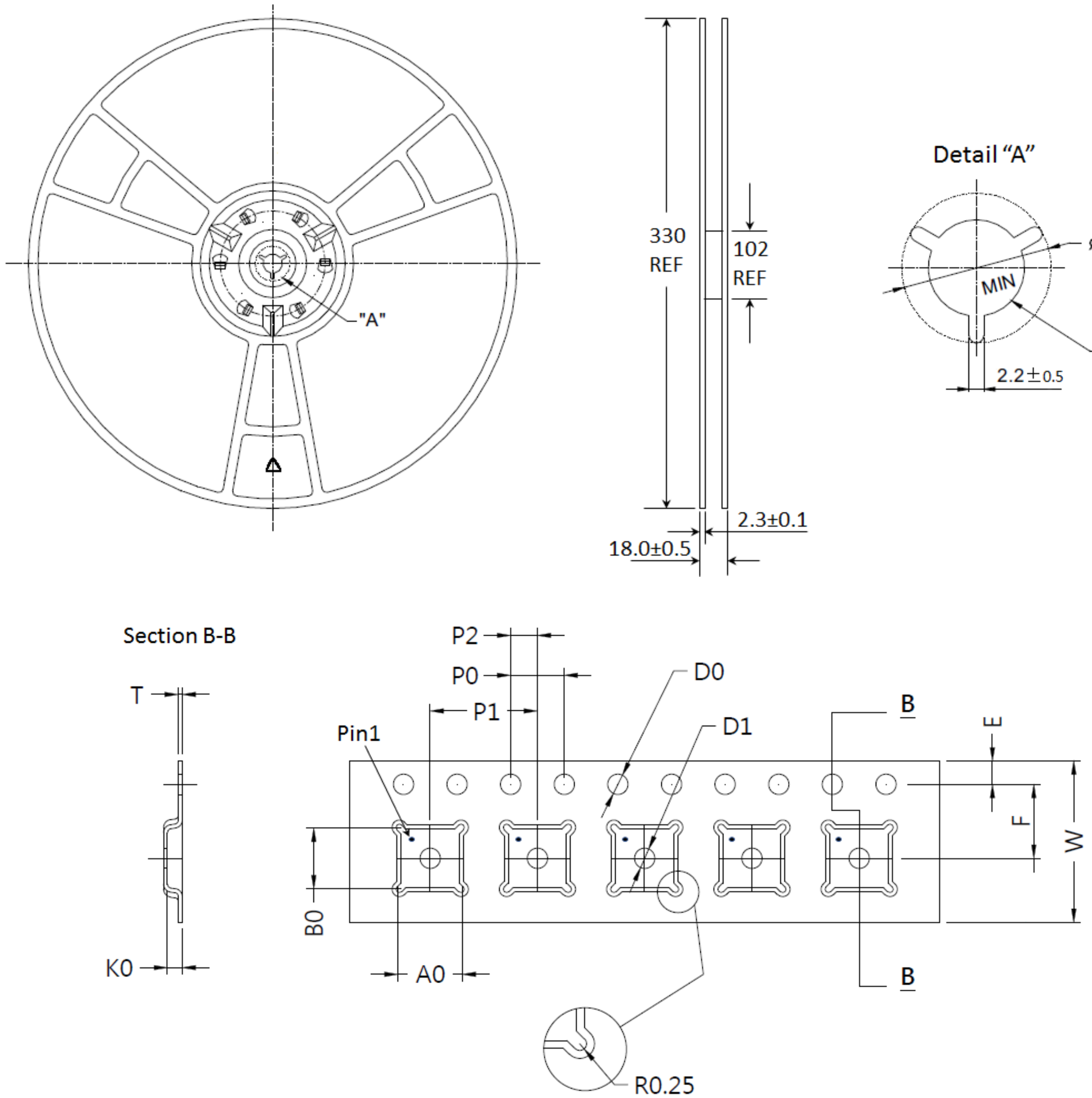

Figure 15.1 Tape and Reel Drawing

Table 15.1 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	3.30	±0.1	K0	1.20	±0.1
B0	6.30	±0.1	P0	4.00	±0.1
D0	1.50	+0.1	P1	8.00	±0.1
D1	1.50	MIN	P2	2.00	±0.1
E	1.75	±0.10	T	0.30	±0.05
F	7.50	±0.10	W	16.00	±3.00

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