TSL8028N: Single channel 2 – 5 GHz 100-Watt Receiver Front End for MACRO base station

1.0 Features

Integrated single-channel RF front end

2-stage LNA and GaN SPDT switch On-chip bias and matching
Single-supply operation

- Gain @ 3.6 GHz: 33 dB [High Gain mode]
  @ 3.6 GHz: 14 dB [Low Gain mode]
- NF @ 3.6 GHz: 1.2 dB [High Gain mode]
  @ 3.6 GHz: 1.1 dB [Low Gain mode]
- OP1dB @ 3.6 GHz: 21 dBm [High Gain mode]
  @ 3.6 GHz: 12 dBm [Low Gain mode]
- Operating frequency: 2 to 5 GHz
- Insertion loss @ 3600 MHz: 0.3 dB [TX mode]
- Switch isolation @ 3.6 GHz: 17 dB [RX HG mode]
- RXHG isolation @ 3.6 GHz: 48 dB [PD=5V & BP=0V]
- RXLG isolation @ 3.6 GHz: 48 dB [PD=BP=5V]
- High power handling at TCASE = 105°C Full lifetime
- LTE average power [8 dB PAR]: 50 dBm
- High OIP3 [high gain mode]: 32 dBm typical
- High gain mode current: 90 mA typical at 5 V
- Low gain mode current: 50 mA typical at 5 V
- Power-down mode current: 4 mA typical at 5 V
- Positive logic control
- 5 mm × 5 mm x 0.85 mm, 32-lead QFN

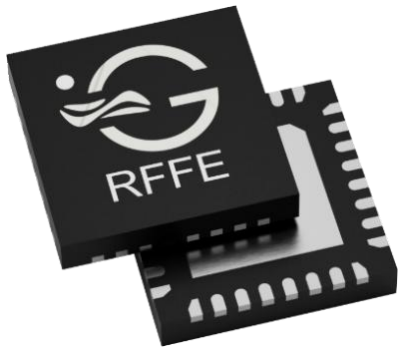


Figure 1.1 Device Image
(5 mm × 5 mm x 0.85 mm, 32-lead QFN)

RoHS/REACH/Halogen Free Compliance

2.0 Applications

- 4G/5G Infrastructure Radios, Macro base station
- Small Cells and Cellular Repeaters
- Phase Array Radar
- SDARS

3.0 Description

The TSL8028N is a single-channel, integrated RF, front-end, multichip module designed for different applications. The device operates from 2 GHz to 5 GHz. The TSL8028N is configured with a cascading, two-stage, GaAs LNA and a GaN based SPDT switch.

In high gain mode, the cascaded two-stage LNA and switch offer a low noise figure of 1.1 dB and a high gain of 33 dB at 3.6 GHz with an output third-order intercept point (OIP3) of 33 dBm (typical) at high gain mode. In low gain mode, one stage of the two-stage LNA is in bypass, providing 14 dB of gain at a lower current of 50 mA. In power-down mode, the LNAs are turned off and the device draws 4 mA.

In transmit operation, when RF inputs are connected to a termination pin (TX), the switch provides low insertion loss of 0.3 dB at 3.6GHz and handles long-term evolution (LTE) average power (8 dB peak to average ratio (PAR)) of 50 dBm for full lifetime operation.

The device comes in a RoHS compliant, compact, 5 mm × 5 mm, 32-lead QFN.

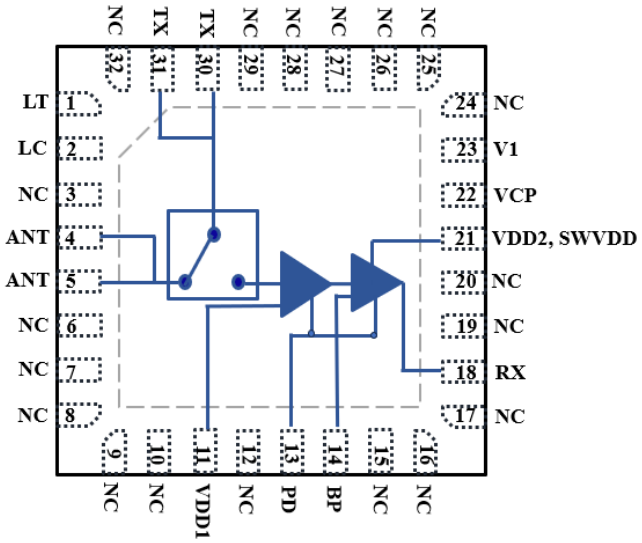


Figure 3.1 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 4.1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TSL8028N	32 Pin 5.0 × 5.0 × 0.85 mm³ QFN	Tape & Reel	3000	13” (330 mm)	18 mm	TSL8028NMTRPBF
Tuned Evaluation Board, 3410-3980 MHz						TSL8028N-EVB-A

5.0 Pin Description

Table 5.1 Pin Definition

Pin Number	Pin Name	Description
1,2	LT, LC	Tuning inductor
3,6,7,8, 9,10,12,15,16,17,19,20, 24,25,26,27,28,29, and 32	NC	Not Internally Connected. It is recommended to connect NIC pins to the RF ground of the PCB.
4,5	ANT	RF Input. The ANT pin is ac-coupled to 0 V and matched to 50Ω. Matching and a dc blocking capacitor are not required.
11	VDD1	Vdd1 supplied through an external choke inductor
13	PD	Power-Down All Stages of LNA
14	BP	Bypass Second Stage LNA
18	RX	Receiver Output. The RX pin is the receiver path for the channel. The RX pin is matched to 50Ω. No matching component is required. A dc blocking capacitor is required.
21	VDD2_ SWVDD	VDD2_SWVDD supplied voltage through an external choke inductor to LNAs and it connected with Supply Voltage for Switch also.
22	VCP	Internal charge pump voltage output. Connect a 1nF capacitor to GND on this pin to improve switching time
23	V1	Control Voltage for Switch.
30,31	TX	Termination Output. The TX pin is the transmitter path. The TX pin is ac-coupled to 0 V and matched to 50Ω. No matching and dc blocking capacitor is required.
Package Base	Paddle/Slug	DC and RF Ground. Also provides thermal relief. Multiple vias are recommended

Note: [1] The backside ground slug of the device must be grounded directly to the ground plane through multiple vias to ensure proper operation. Adequate heatsink required.

6.0 Absolute Maximum Rating

Table 6.1 Absolute Maximum Rating @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Supply voltage, VDD1, VDD2, SWVDD	V_{dd}	+5.5	V
RF input power Transmit Input Power (LTE Peak, 8 dB PAR) Receive Input Power (LTE Peak, 8 dB PAR)	RF_{IN}	 58 25	 dBm dBm
Digital Control Input Voltage V1, BP and PD		2.6 to 5.5	V
Digital Control Input Current V1, BP and PD		0.2	mA
Storage Temperature Range	T_{st}	-55 to +150	°C
Operating Temperature Range	T_{op}	-40 to +105	°C
Maximum Junction Temperature	T_J	170	°C
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	15.0	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Recommended DC Operating Conditions

Table 7.1 Recommended Operating Conditions @ T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Drain Voltages	VDD1		+5.0		V
	VDD2		+5.0		
Drain Bias Currents	I_{DQ1}, Set by external drain feed		50		mA
	I_{DQ2}, Set by external drain feed		90		
Switch Supply	SWVDD		+5		V
Switch Control Voltages	V1, BP and PD	-0.3		+5.5	V
RF Input Power in Tx mode At ANT	V1 = 5 V, PD = 5 V, BP = 0 V, 8 dB PAR LTE full lifetime average		50		dBm
	V1 = 5 V, PD = 0 V, BP = 0 V, 8 dB PAR LTE full lifetime average			TBD	dBm
	V1 = 5 V, PD = 0 V, BP = 5 V, 8 dB PAR LTE full lifetime			TDB	dBm
Digital Inputs	V1, PD Low (VIL) High (VIH)	 -0.3 2.6		 0.5 Vdd	V
	BP Low (VIL) High (VIH)	 0 2.6		 0.5 Vdd	
Digital Input Currents	V1 [=5 V]			<7.5	µA
	PD [=5 V]			200	
	BP [=5 V]			100	
Switch control max current				7.5	µA
Operating Temperature Range	T_{op}	-40	+25	+105	°C

Table 7.2 Truth Table: Switch control

V1(Switch control)	Signal Path Select	
	Transmit Operation	Receive Operation
Low	Off	On
High	On	Off

Table 7.3 Truth Table: Receive Operation

Receive Operation	PD	BP	Signal Path
High Gain Mode	Low	Low	ANT to RX
Low Gain Mode	Low	High	
Power-Down Mode [LNA is on HG]	High	Low	
Power-Down Mode [LNA is on LG]	High	High	

8.0 RF Electrical Specifications for EVBs

VDD1, VDD2_SWVDD = 5 V, BP= 0 V / 5 V and PD=0 V TCASE = 25°C, and 50 Ω system, unless otherwise noted.

Table 8.1 3410 – 3980 MHz EVB A

Parameter		Test Condition	Minimum	Typical	Maximum	Unit
Operational frequency			3.41		3.98	GHz
Gain		LNAs on Bypass off (High gain)		30.8-33.5		dB
		LNA1 on Bypass on (Low gain)		13.3-14.6		dB
Noise Figure	(De-embedded)	LNAs on Bypass off (High gain)		1.2		dB
		LNA1 on Bypass on (Low gain)		1.1		dB
	[SMA-SMA]	LNAs on Bypass off (High gain)		1.4		dB
		LNA1 on Bypass on (Low gain)		1.3		dB
Input Return Loss		LNAs on Bypass off (High gain)		< -11		dB
		LNA1 on Bypass on (Low gain)		< -17		dB
Output Return Loss		LNAs on Bypass off (High gain)		< -8.7		dB
		LNA1 on Bypass on (Low gain)		< -10.5		dBm
OP1dB		LNAs on Bypass off (High gain)		19-21		dBm
		LNA1 on Bypass on (Low gain)		8.5-13		dBm
OIP3		LNAs on Bypass off (High gain) 0 dBm/tone, Tone Spacing 1 MHz		31-33		dBm
		LNA1 on Bypass on (Low gain) 0 dBm/tone, Tone Spacing 1 MHz		18-24		dBm
Current, Id		LNAs on Bypass off (High gain)		93		mA
		LNA1 on Bypass on (Low gain)		52		
		PD mode ON (Both LNAs OFF)		4		
Insertion Loss	[SMA-SMA]	Transmit operation		0.6-0.7		dB
	[De-embedded]	Transmit operation		0.3-0.4		dB
ANT-TX Isolation, RX-LG mode		V1=0 V, VDD1, VDD2= 5 V, PD=0 V, BP= 5 V Port ANT-TX		>20		dB

ANT-TX Isolation, RX-HG mode	V1=0 V, VDD1, VDD2= 5 V, PD=0 V, BP= 0 V Port ANT-TX		>17		dB
ANT-RXLG Isolation, TX mode	V1=5 V, VDD1, VDD2= 5 V, PD=5 V, BP= 5 V Port ANT-RX		>44		dB
ANT-RXHG Isolation, TX mode	V1=5 V, VDD1, VDD2= 5 V, PD=5 V, BP= 0 V Port ANT-RX		>45		dB

Table 8.2 TX Switching Speed

Parameter	Test Condition	Switching time[ns]	Mode
SWITCHING CHARACTERISTICS (t_{ON}, t_{OFF})	50% Ctrl → 10 % RF RX	1400	TX/RX mode
	50% Ctrl → 90 % RF TX	1500	
	50% Ctrl → 10 % RF TX	1900	
	50% Ctrl → 90 % RF RX	1600	

Table 8.3 RX Switching Speed

Pin toggle	State		Switching time[ns]	Mode	DC Condition
BP	LG to HG		200 ns	RX mode	VDD2_SWVDD=5 V, V1=5 V, VDD1=5 V, PD=0 V
	HG to LG		450 ns		
PD	Low Gain	On to Off	360 ns	RX-LG mode	VDD2_SWVDD=5 V, V1=5 V, VDD1=5 V, PD=0 V & BP=0 V
		Off to on	450 ns		
	High Gain	On to Off	360 ns	RX-HG mode	VDD2_SWVDD=5 V, V1=5 V, VDD1=5 V, PD=0 V & BP=5 V
		Off to on	720 ns		

9.0 Typical performance characteristics of TSL8028N EVB A

9.1 Receive Operation, Low Gain Mode 3.41-3.98 GHz tuned EVB

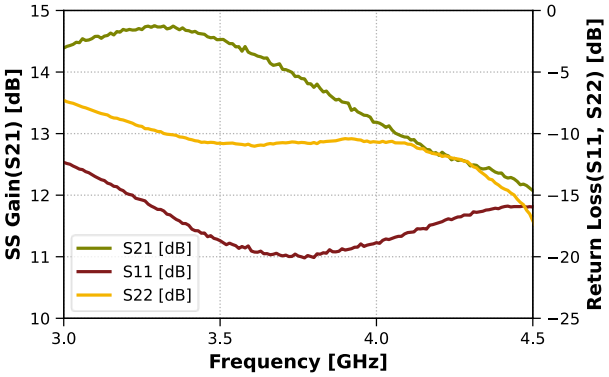


Figure 9.1.1 Scattering Parameters vs Frequency (Narrow band)

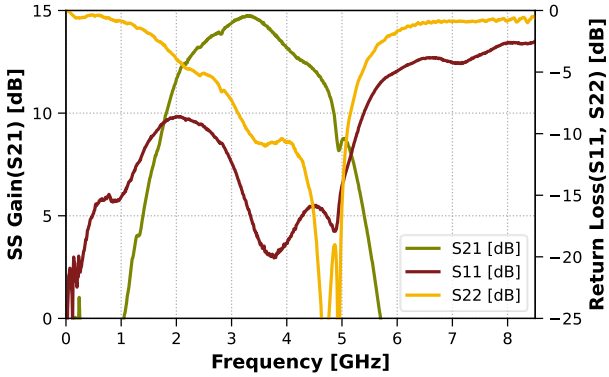


Figure 9.1.2 Scattering Parameters vs Frequency (wide band)

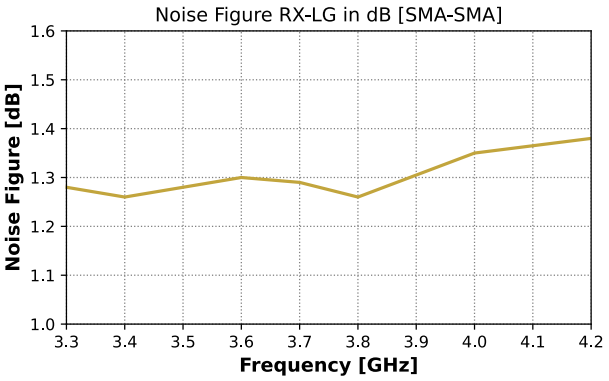


Figure 9.1.3 Noise Figure vs Frequency

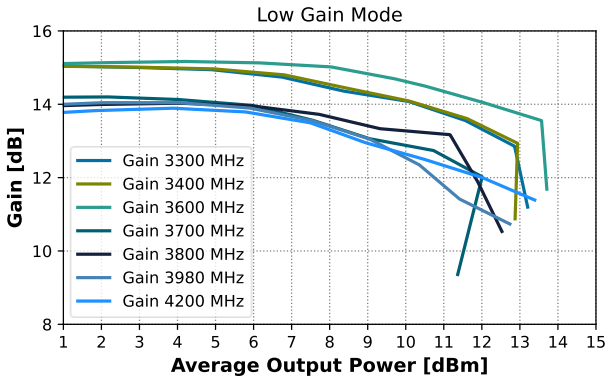


Figure 9.1.4 Gain vs Pout

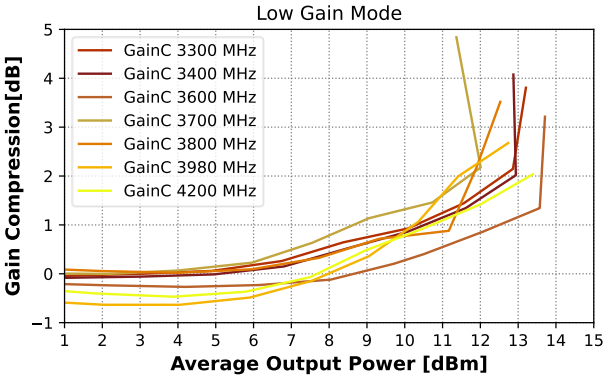


Figure 9.1.5 Gain Compression vs Pout

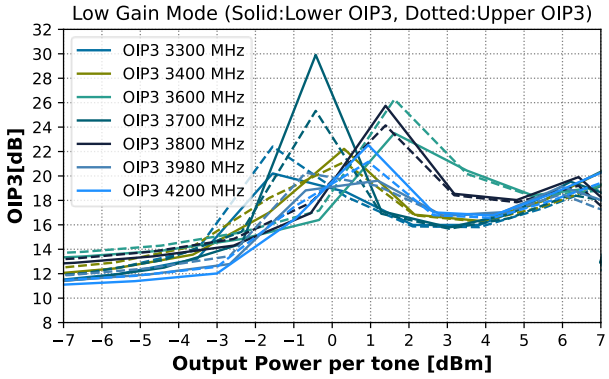


Figure 9.1.6 OIP3 vs Output Power/tone

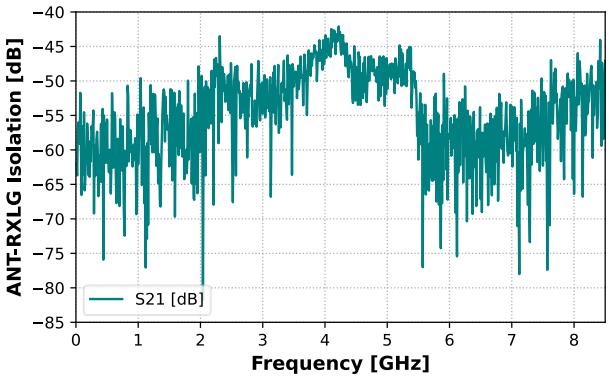


Figure 9.1.7 ANT-RXLG Isolation, TX mode : V1=5 V, VDD1, VDD2= 5 V, PD=5 V, BP= 5 V Port ANT-RX

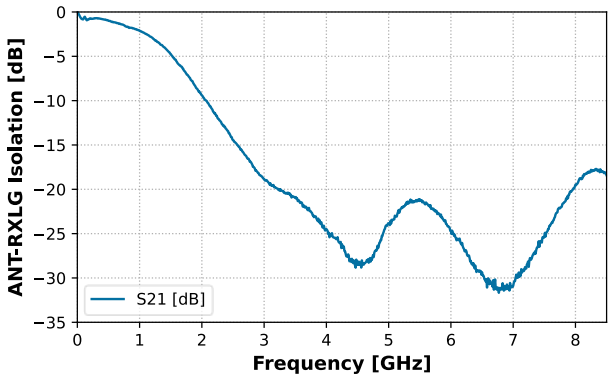


Figure 9.1.8 ANT-TX Isolation, RXLG Mode : V1=0 V, VDD1, VDD2= 5 V, PD=0 V, BP= 5 V Port ANT-TX

9.2 Receive Operation, High Gain Mode 3.41-3.98 GHz tuned EVB A

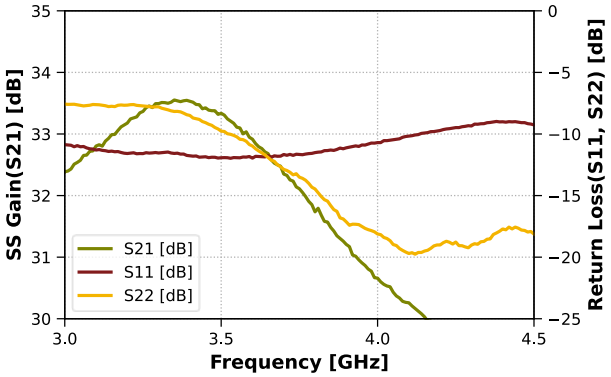


Figure 9.2.1 Scattering Parameters vs Frequency (Narrow band)

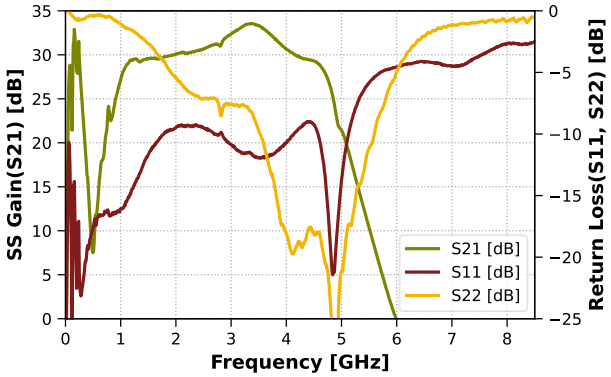


Figure 9.2.2 Scattering Parameters vs Frequency (wide band)

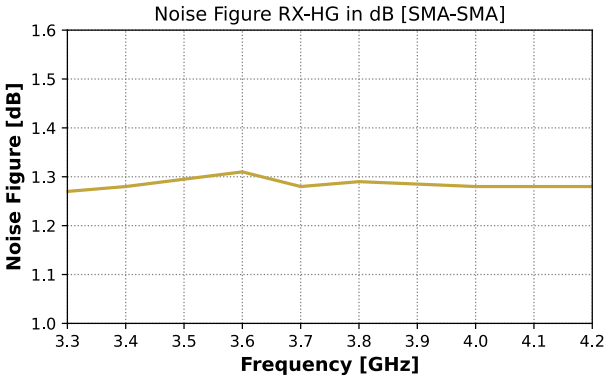


Figure 9.2.3 Noise Figure vs Frequency

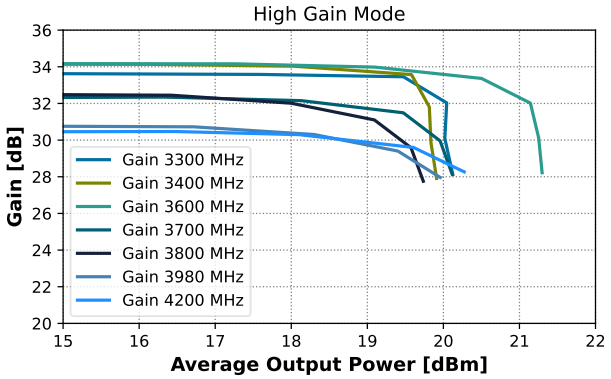


Figure 9.2.4 Gain vs Frequency

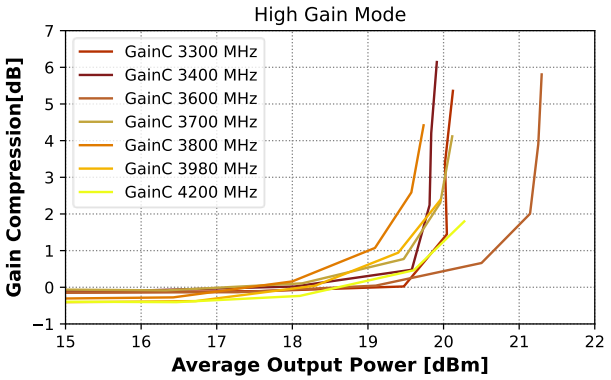


Figure 9.2.5 Gain Compression vs Pout

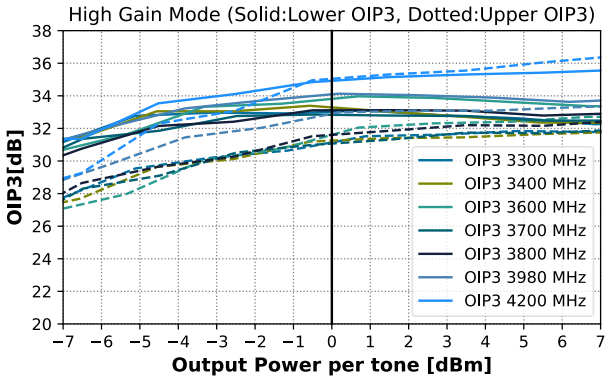


Figure 9.2.6 OIP3 vs Output Power/tone

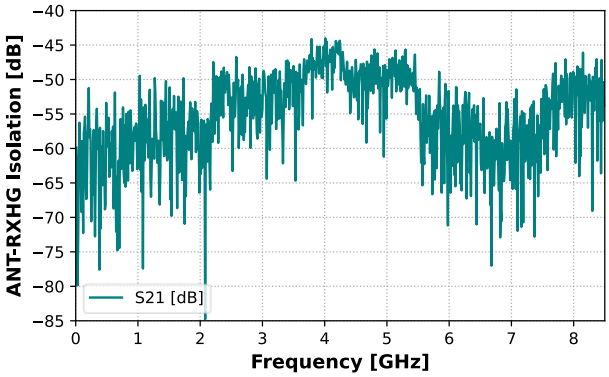


Figure 9.2.7 ANT-RXHG Isolation, TX mode, V1=5 V, VDD1, VDD2= 5 V, PD=5 V, BP= 0 V Port ANT-RX

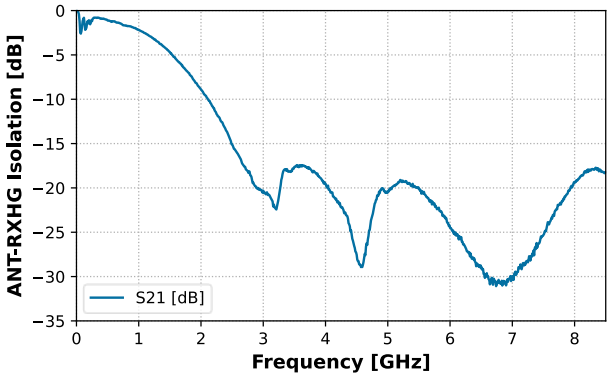


Figure 9.2.8 ANT-TX Isolation, RXHG Mode V1=0 V, VDD1, VDD2= 5 V, PD=0 V, BP= 0 V Port ANT-TX

9.3 Transmit Mode 3.41-3.98 GHz tuned EVB A

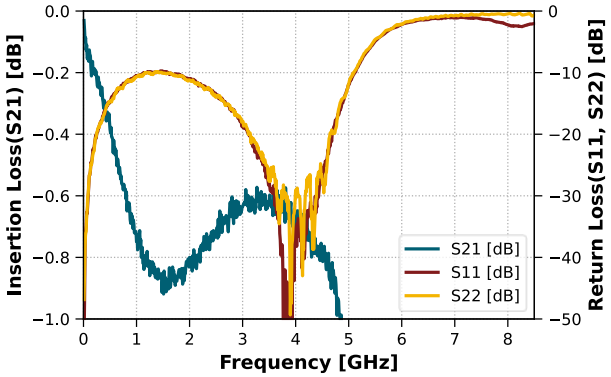


Figure 9.3.1 Scattering Parameters vs Frequency

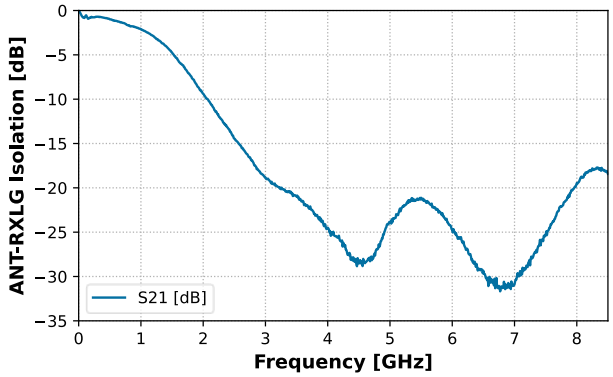


Figure 9.3.2 ANT-TX Isolation, RXLG Mode V1=0 V, VDD1, VDD2= 5 V, PD=0 V, BP= 5 V Port ANT-TX

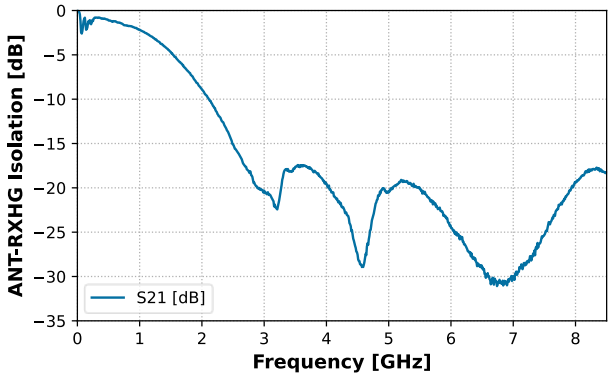


Figure 9.3.3 ANT-TX Isolation, RXHG Mode V1=0 V, VDD1, VDD2= 5 V, PD=0 V, BP= 0 V Port ANT-TX

10.0 Evaluation Boards

10.1 3410-3980 MHz EVB A

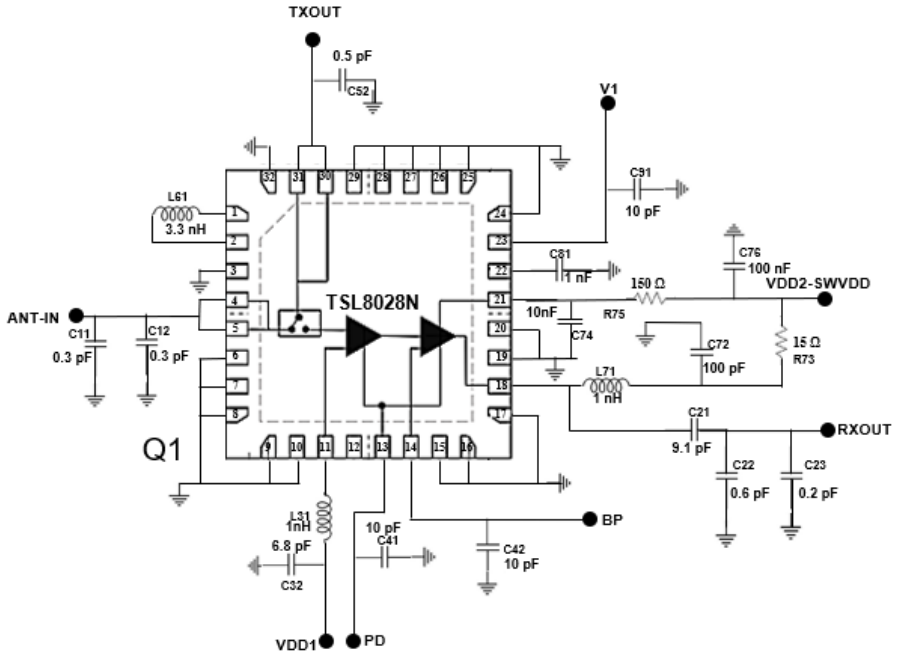


Figure 10.1.1 Schematic of the 3410-3980 MHz EVB A

Table 10.1.1 BOM of the 3410-3980MHz EVB A

Component ID	QNTY	Value	Case Code [in]	Manufacturer	Recommended Part Number
C11, C12	2	0.3pF	0603	Murata	600S0R3BT250XT
C21	1	9.1pF	603	Murata	600S9R1BT250XT
C22	1	0.6pF	0402	Murata	GJM1555C1HR60BB01J
C23	1	0.2pF	0402	Murata	GJM1555C1HR20BB01J
L31, L71	2	1nH	0402	Coil craft	0402DC-1N0XJRW
C32	1	6.8pF	0402	Murata	GJM1555C1H6R8BB01D
C41, C42, C91	3	10pF	0402	Murata	GJM1555C1H100JB01D
C52	1	0.5pF	0603	Murata	600S0R5BT250XT
L61	1	3.3nH	0402	Coil craft	0402DC-3N3XGRW
C72	1	100pF	0402	AVX	04025A101JAT4A
R73	1	15Ω	0402	Panasonic	ERJ-H2RD15R0X
C74	1	10nF	0402	AVX	04025C103K4T2A
R75	1	150Ω	0402	Panasonic	ERJ-2RHD1500X
C76	1	100nF	0402	TDK	C1005X7R1H104K050BE
C81	1	1nF	0402	Murata	04025C102JAT2A
Q1	1			TagoreTech	TSL8028N
PCB	1	Rogers RO4350B, 20 mils, 1 oz copper			

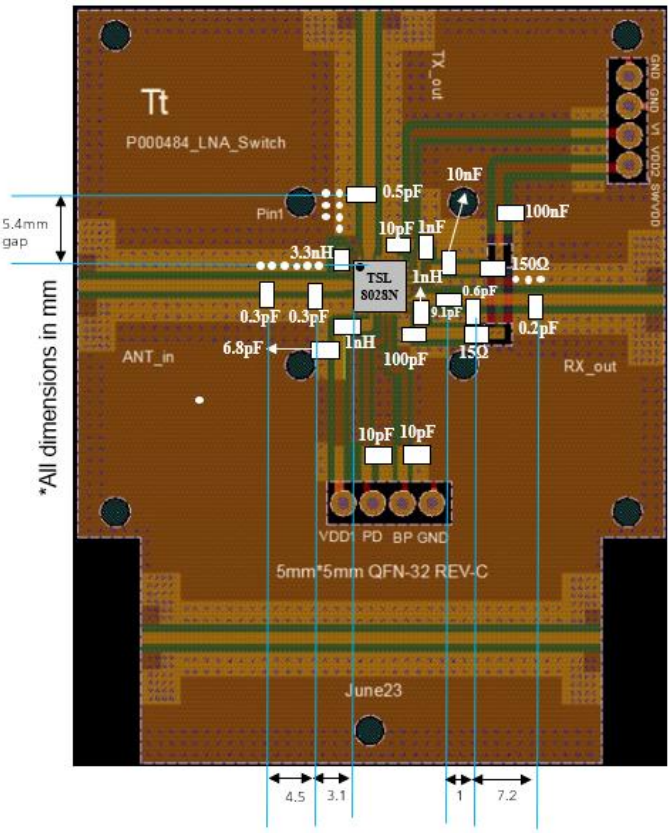
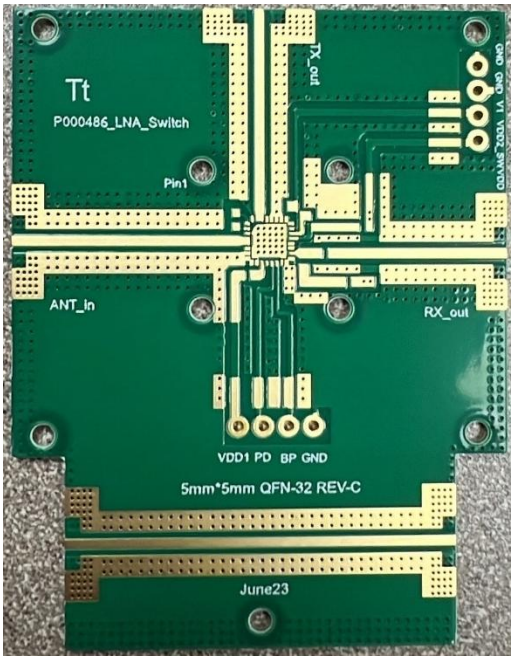


Figure 10.1.2 Layout of the 3410-3980 MHz EVB A

Note: Series cap on ANT and TX ports should have 250 V voltage ratings to handle 100 W power.

The heatsink needs to be added at bottom of this board for proper power spreading.



11. Test Procedure

Biasing sequence

To properly bias the TSL8028N-EVB-A, follow these steps:
Ground the Gnd test point.

- Apply bias to the VDD2_SWVDD and VDD1=5 V test points.
- Apply bias to the V1 test point.
- Apply bias to the BP test points.
- Apply bias to the PD test point.
- Apply an RF input signal.

The TSL8028N-EVB-A is shipped fully assembled and tested. Figure 11.1 illustrates a basic test setup diagram for evaluating s-parameters in RX mode, including receive gain, transmit insertion loss and isolation, and RF input and output return losses using a network analyzer. Follow these steps to complete the test setup and verify the operation of the TSL8028N-EVB-A:

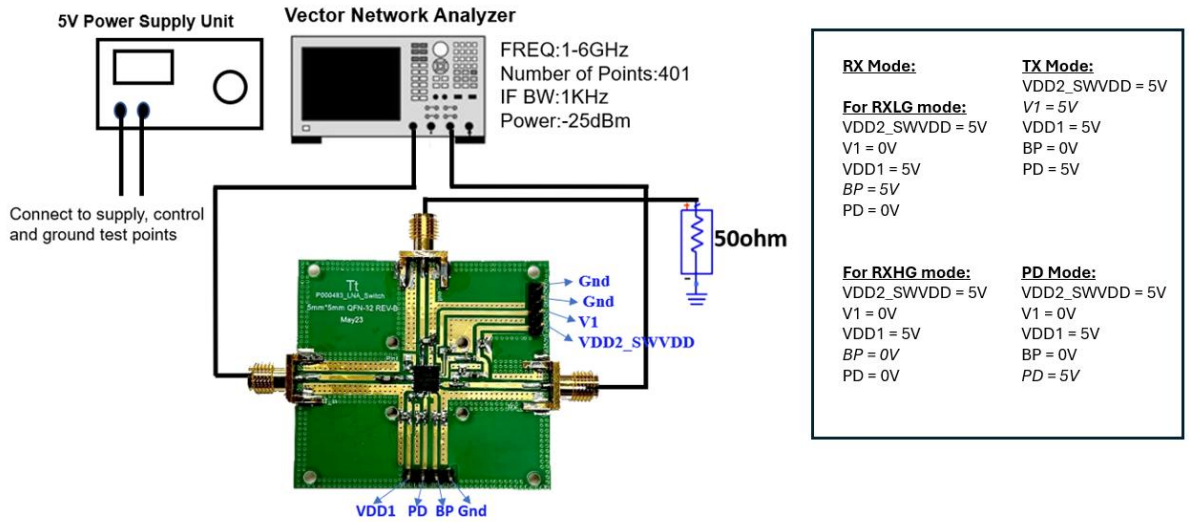


Figure 11.1 Test set up for different modes

1. Connect the Gnd test point to the ground terminal of the power supply.
2. Connect the Vdd1, SWVDD and Vdd2 test points to the voltage output terminal of a 5 V supply that sources a current of approximately 90 mA in receive operation for high gain mode, 50mA in receive operation in low gain mode and 4-5 mA for power-down mode.
3. Connect the BP, PD, and V1 test points to the ground terminal of the power supply for high gain receive operation.
4. Connect the PD, and V1 test points to the ground terminal & BP to 5V of the power supply for low gain receive operation.
5. The TSL8029-EVB-A can be configured in different modes by connecting the control test points to 5 V or ground, as shown in Table 7.2 and Table 7.3.
6. Connect a calibrated network analyzer to the ANT_in, TX_out, and RX_out SMA connectors. Sweep the frequency from 1 GHz to 6 GHz and set the power to -25 dBm.

TSL8028N-EVB-A is expected to have a high and low receive gain of 33 dB and 14 dB respectively at 3.6 GHz. Refer Figure 9.1.1 & Figure 9.2.1 for the expected results.

Additional test equipment is required for a comprehensive evaluation of the device's functions and performance.

For noise figure evaluation, use either a noise figure analyzer or a spectrum analyzer with a noise option. It is recommended to use a low excess noise ratio (ENR) noise source.

For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high isolation power combiner is recommended.

For power compression and power handling evaluations, use a two-channel power meter and a signal generator. Ensure that the input power amplifier has sufficient power capacity. Test accessories such as couplers and attenuators must also have adequate power handling capabilities.

The TSL8028N-EVB-A is equipped with a support plate attached to the bottom side. To ensure optimal heat dissipation and minimize thermal rise during high power evaluations, attach this support plate to a heat sink using thermal grease.

Please note that measurements conducted at the SMA connectors of the TSL8028N-EVB-A include the losses of the SMA connectors and the PCB. The through-line should be measured to calibrate the effects of the TSL8028N-EVB-A. The through line consists of an RF input line and an RF output line that are connected to the device and have equal lengths. The through line information is provided in the EVB.

12.0 Device Package Information

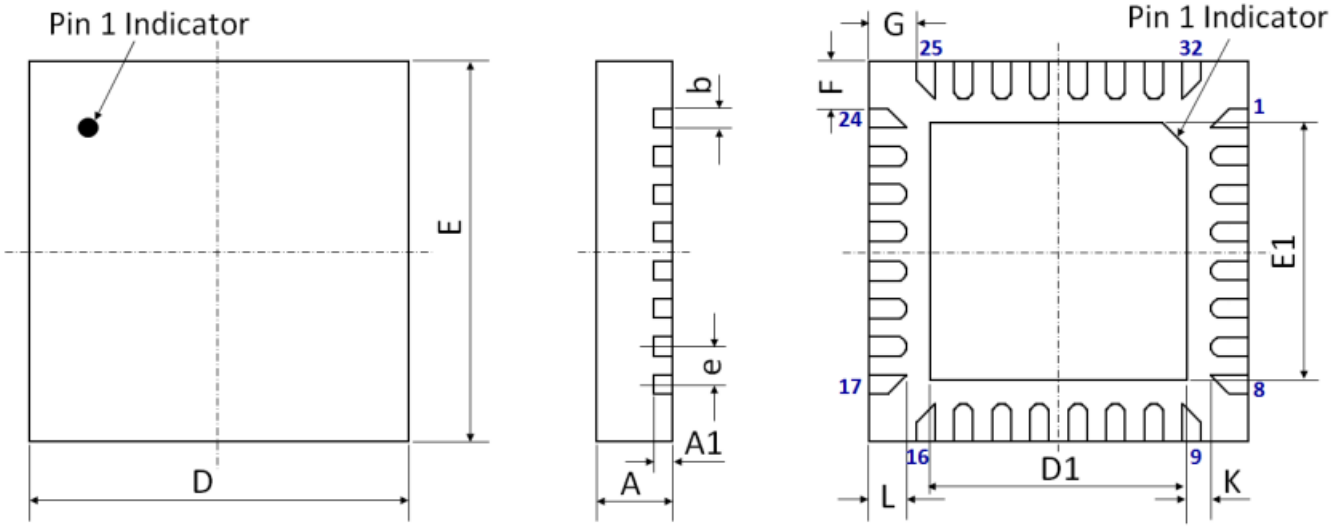


Figure 12.1 Device Package Drawing
(All dimensions are in mm)

Table 12.1 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.85	±0.05	E	5.00 BSC	±0.05
A1	0.203	±0.02	E1	3.2	±0.06
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	5.00 BSC	±0.05	G	0.625	±0.05
D1	3.2	±0.06	L	0.40	±0.05
e	0.5 BSC	±0.05	K	0.5	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5 µm ~ 20 µm (Typical 10 µm ~ 12 µm)

Attention:

Please refer to application notes *TN-001* and *TN-003* at http://www.tagoretech.com/ for PCB and soldering related guidelines.

13.0 PCB Land Design

Guidelines:
[1] 4-layer PCB is recommended.
[2] Via diameter is recommended to be 0.2 mm to prevent solder wicking inside the vias.
[3] Thermal vias shall be placed on the center pad and should be filled/plugged with solder or copper.
[4] The maximum via number for the center pad is 5(X)×5(Y)=25.

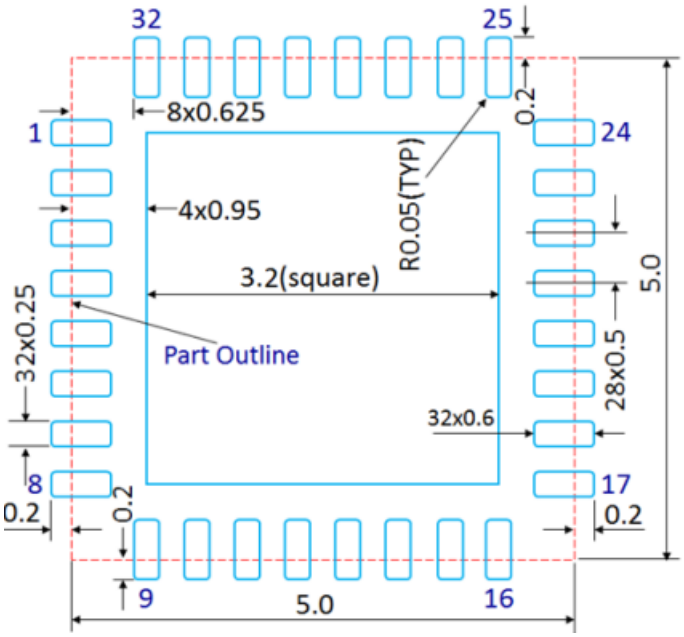


Figure 13.1 PCB Land Pattern
(Dimensions are in mm)

Non-Solder Mask Defined (Preferred) Solder Mask Defined

Figure 13.2 Solder Mask Pattern
(Dimensions are in mm)

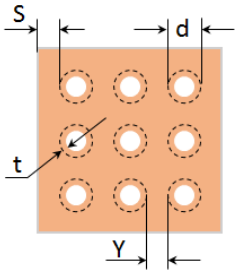


Figure 13.3 Thermal Via Pattern
(Recommended Values: S≥0.15 mm; Y≥0.20 mm; d=0.3 mm; Plating Thickness t=25 µm or 50 µm)

14.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125 µm.

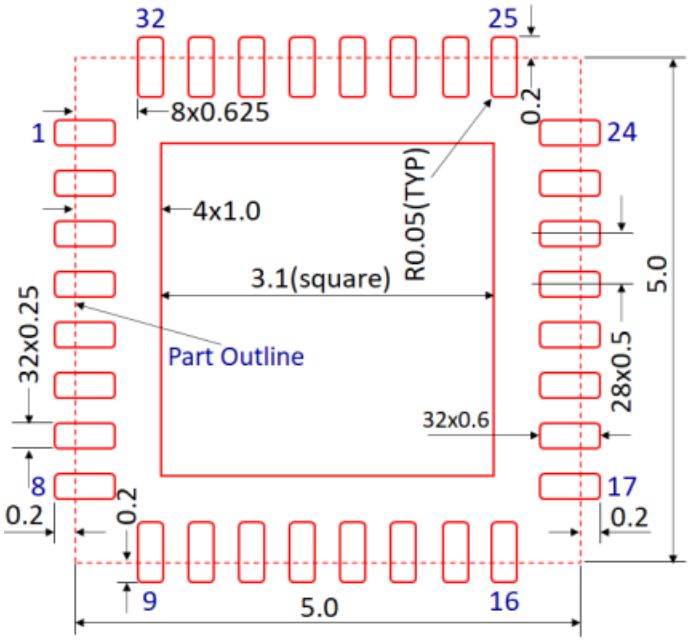


Figure 14.1 Stencil Openings
(Dimensions are in mm)

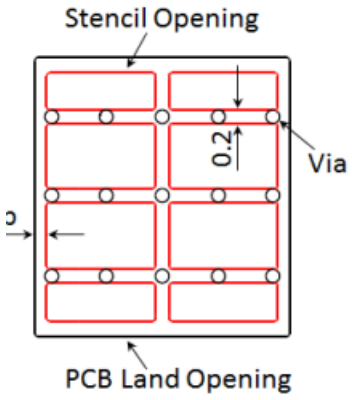


Figure 14.2 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

15.0 Tape and Reel Information

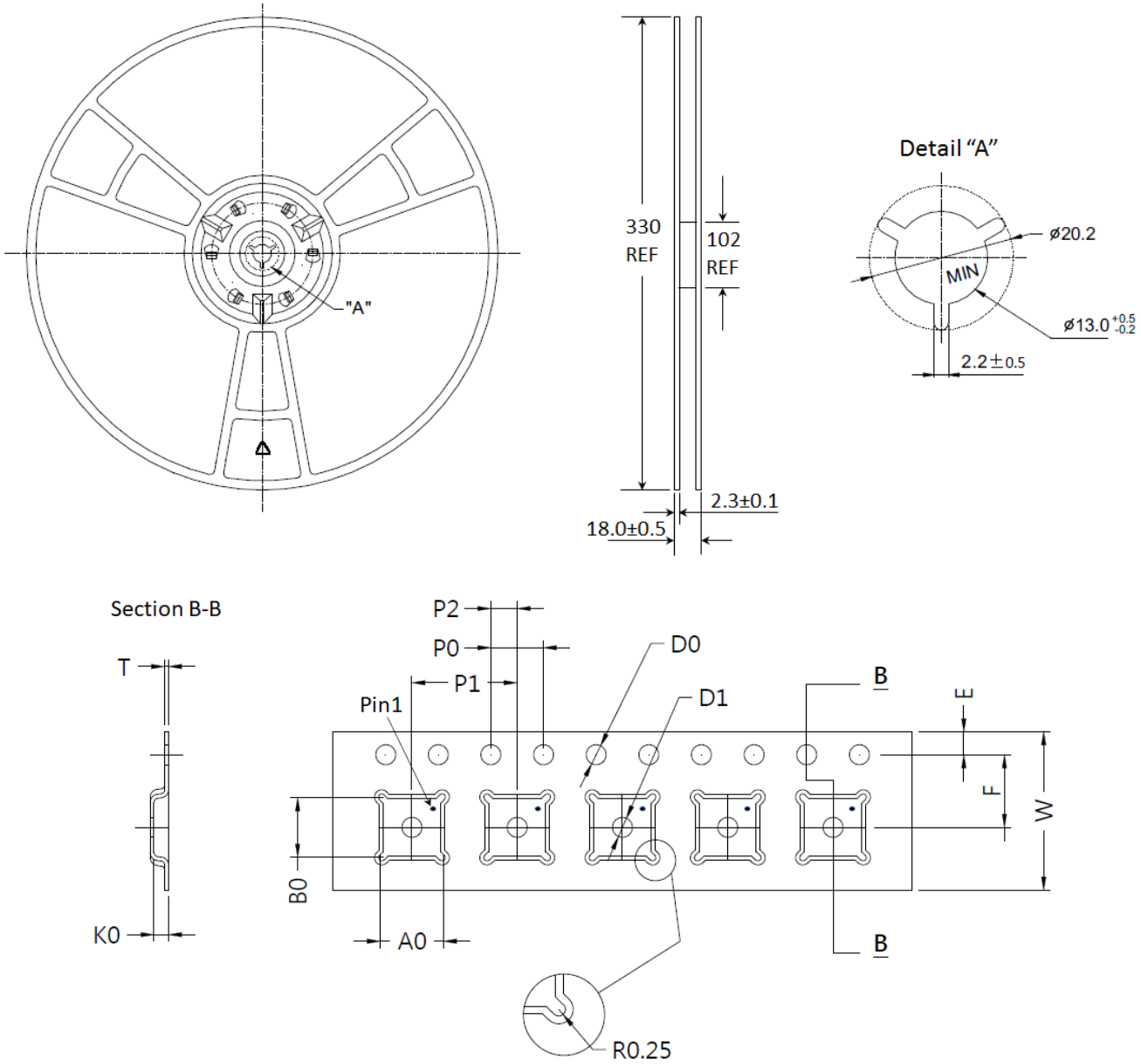


Figure 15.1 Tape and Reel Drawing

Table 15.1 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	5.35	±0.10	K0	1.10	±0.10
B0	5.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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